Reduction of Clock Power in Sequential Circuits Using Multi-Bit Flip-Flops

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Abstract— **Power reduction plays a vital role in VLSI design. Multi-bit flip-flop is an efficient method for clock power reduction. This method is to eliminate the redundant inverters by merging some flip-flops into multi-bit flip-flops. This multi-bit flip-flops can share the drive strength, dynamic power, area of the inverter chain and can even save the clock network power and facilitate the skew control. Firstly flip-flops that can be merged are identified based on synchronous clock signal and then a combination table is built to define the possible combination of flip-flops and finally a hierarchical way is used to merge flip-flops.**

Index Terms— Dynamic power, multi-bit flip-flop, merging, redundant inverters

I. INTRODUCTION

In modern IC design, the power consumption of the clock network plays a major role in whole design especially for scaled CMOS technologies. The clock distribution network consumes the 75% of thermal power which is the major contributor to the dynamic power of the chip due to its highest switching rate. Nowadays, reducing the power consumption is a tedious process in IC fabrication. In design, the power consumption can be optimized by using several methodologies such as minimizing clock networks [1], creating multi-supply-voltage (MSV) designs and using multi-bit registers . In this paper, the concept of multi-bit flip-flops (MBFFs) are used to reduce the power consumption of the clock network connected to the flip-flops. However, to apply MBFFs in early design, it is difficult to consider the trade-off among power and timing. Therefore, the power consumption of flip-flops is reduced by applying MBFFs at the post placement stage [2]-[5].

Multi-bit flip-flop
Multi-bit flip-flop is defined as the merging of multiple single bit flip-flops. Thus a single bit flip-flop has two latches called master latch and slave latch.
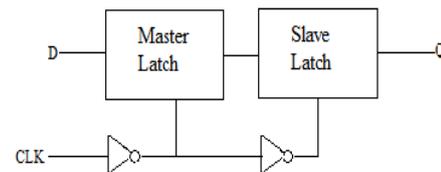

Figure 1: Single bit Flip-Flop

These latches need the clock signal to perform the operation. Figure 1 shows an example of single bit flip-flop. In order to provide better delay from clk_Q, two inverters are used in the clock path signal. Thus the clock signal is regenerated from clock. By merging several single bit flip-flops total inverters in the circuit are reduced, hence the power consumption and area also reduced. Figure 2 shows an example of merging two 1-bit flip-flops into 2-bit flip-flop. Thus each 1-bit flip-flop contains two inverters called master latch and slave latch.
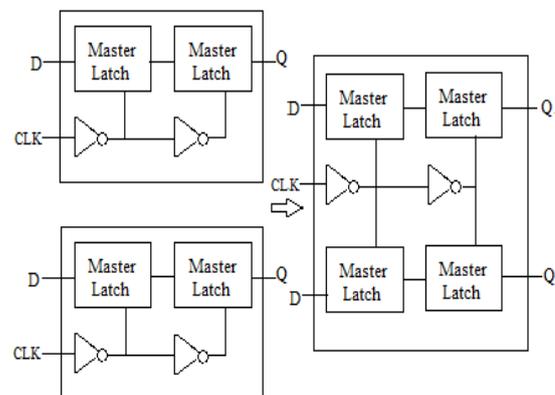

Figure 2: Example of merging two 1-bit flip-flops into 2-bit flip-flop

Due to the manufacturing rules, the size of the inverters tends to be oversized. As the process technology progresses, the minimum size of clock buffers can drive more than one flip-flop. Thus merging single bit flip-flops into multi-bit flip-flop can avoid the redundant inverters and lower the clock power consumption. Thus the total area of the circuit is also

reduced. By using this method in ASIC design, following benefits are provided.

- Duplicate inverters are avoided
- Total area of flip-flop can be reduced
- Power reduction through shared inverters
- Clock skew can be controlled because of the common clock signal

Based on the driving strength of the minimum sized inverter on given rising or falling time, the driving capability of a clock buffer can be calculated. The paper is organized as follows. Section II discusses design flow of flip-flop merging and Section III discusses power optimization technique. Section IV gives the simulation result with discussion of clock power reduction.

II. DESIGN FLOW

Design flow has three consecutive steps to minimize the power consumption of clock network and also avoid the wastage of time in finding the impossible combination of flip-flops. As shown in the figure 3 the first step is transformation of placement space which is used to identify the overlapped area of flip-flops. Then the flip-flops that are going to be merged are easily identified. The second step is build combination table which is used to avoid time wasting in finding impossible combination of flip-flops.
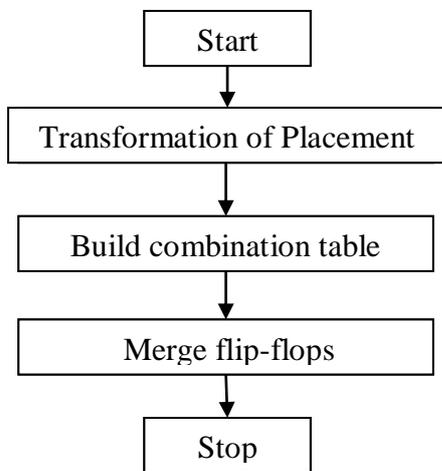

Figure 3: Design Flow

The combination table is used to provide the possible combination of flip-flops which are going to be merged. The third step is flip-flop merging. In this step, the chips are divided into the several bins and flip-flops are merged in different bin. This step is repeated until all the possible flip-flops are merged.

Transformation of Placement Space

The feasible placement region of each and every flip-flop can be identified with the help of Manhattan distance as shown in the figure 4. In Manhattan routing model, the collection of points within a fixed distance is called Manhattan circular region whose boundary is composed of to line segments with the slope +1 and two line segments -1. Thus the feasible location region of 1-bit flip-flop is obtained by the intersection of two Manhattan circular regions. Then the legal placement region of new flip-flop can be identified by the overlapped area of several regions of the flip-flop. However the placement region of the flip-flop is in diamond shape, it is difficult to identify the overlapped regions of the flip-flops. Therefore the overlapped area can be identified more easily if the coordinate system of cells is transformed to get rectangular regions. Thus the transformation of placement space is the easiest way to identify overlapped region of the flip-flops.
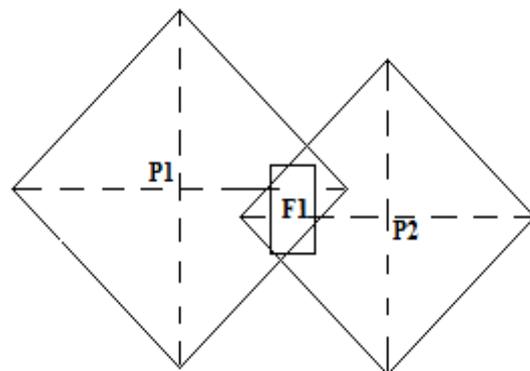

Figure 4: Feasible location region for 1-bit flip-flop

The feasible location region of the new flip-flop is obtained by the overlapping region of several flip-flops. Figure 5 shows an example of overlapping region of two flip-flops (f1 and f2). Then the new flip-flop is used to replace the flip-flops f1 and f2.
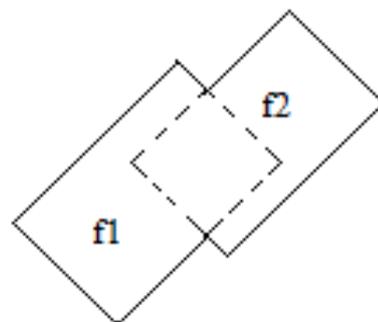

Figure 5: overlapping region of f1 and f2

The overlapping region of flip-flops f1 and f2 are in diamond shape. Hence it is difficult to identify the overlapping region because if the shapes are diamond, four coordinates are required to obtain the overlapping region. In order to overcome this, each segment is rotated by 450, and then the shapes of all the regions become rectangular. In such condition, only two coordinates are required to obtain the overlapping regions.
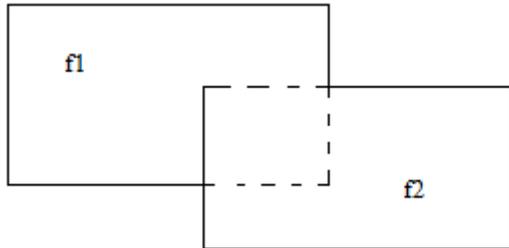

Figure 6: Rotating the diamond shapes by 450

As shown in the figure 6, the rectangular regions are obtained by rotating the legal placement region of the flip-flops f1 and f2 by 450.

Build Combination table

If several flip-flops are replaced by the new flip-flop, it is necessary to ensure that the new flip-flop is provided by the library L. In that case, the combination table is built which defines the possible combinations of flip-flops to get new flip-flops before replacement.
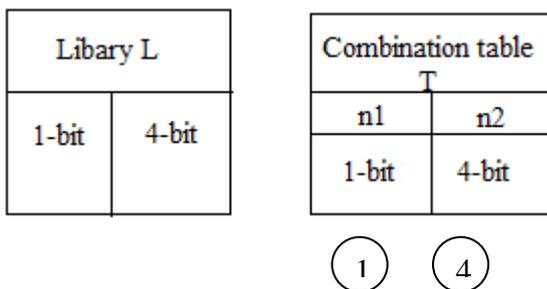

Figure 7(a): Initialize the library and corresponding binary tree is built for each combination in T

The library is initialized to store the possible combination of flip-flops in digital circuits as shown in the figure 7(a). Then the combination table is built to identify the flip-flops which are going to be merged. Additional flip-flops are also added in library.

Library L			
1-bit	2-bit (Pseudo type)	3-bit (Pseudo type)	4 bit

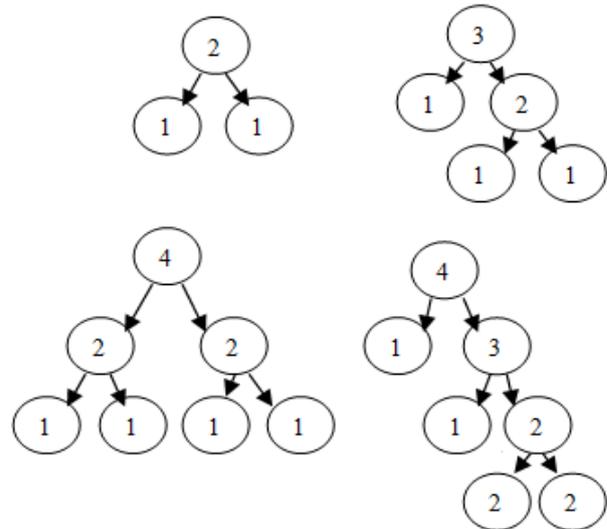| Combination table T					
n1	n2	n3	n4	n5	n6
1-bit	4-bit	2-bit (n1+n1)	3-bit (n1+n3)	4-bit (n3+n3)	4-bit (n1+n4)

Figure 7(b): Pseudo types are added in the library and corresponding binary tree

As shown in the figure 7(b), the pseudo types (1-bit and 2-bit) are added into the library. Then the corresponding binary tree is constructed for each kind of flip-flop. For 4-bit flip-flop, two combinations are possible with that only one combination is used based on the feasible location. If there is any unused combination, then it will be deleted from the table.

Merge Flip-Flops

The Combination table is used to merge the flip-flops. In order to reduce the complexity, the whole placement region of the circuit is divided into several regions and the combination table is used to merge the flip-flops in each subregion. Then, these subregions are combined to form large subregion and flip-flops are merged again so that the flip-flops in near subregions are merged further.

There are several steps to merge flip-flops. They are
Divide the chip into regions
Replace flip-flops in each subregion
Subregions are combined and replace flip-flops
De-replace and replace flip-flops

After de-replacing, the replacement of flip-flops is done according to the combination table T without considering the combinations which corresponds to the pseudo type in library L. The core is to seek the suitable combinations of flip-flops

continuously until it finds the optimized solutions from all possibilities. Thus the procedure of flip-flop merging depends on the combination table, which continuously records the combination among the flip-flop types.

III. POWER OPTIMIZATION TECHNIQUE

The approach called clock gating will be used to reduce the power consumption and also increases the number of flip-flops to be merged. The clock gating technique is used to avoid unnecessary power consumption like the power wasted by timing components when the system is in idle state. Specifically for flip-flops, clock gating means disabling the clock signal when the input data does not alter the stored data. It can be applied where the entire functional unit is set into sleep mode.

Each clock input of a flip-flop can be disabled individually, yielding maximum clock separation and results in high overhead. Thus the clock disabling circuit is shared by a group of several flip-flops in an attempt to reduce the overhead. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In this technique, clock is selectively stopped for the portion of the circuit which is not performing any active computation. An example of a gated clock is shown in the figure 8.In this figure, the power consumption is reduced by inserting the and gate before the latch.
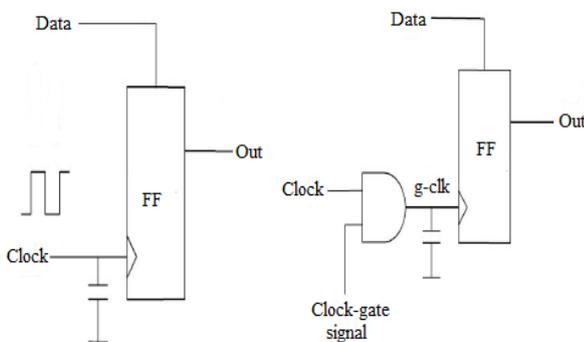

Figure 8: Clock gating implementation in latch

III. RESULT ANALYSIS

The concept is implemented using verilog language and executed by Quartus II IDE with Modelsim simulator. The flip-flops are merged in order to reduce the unnecessary

power wastage through the use of multiple clock sinks. Figure 9 shows the combination table is built for merging the flip-flops. Figure 10 shows the flip-flop merging output.
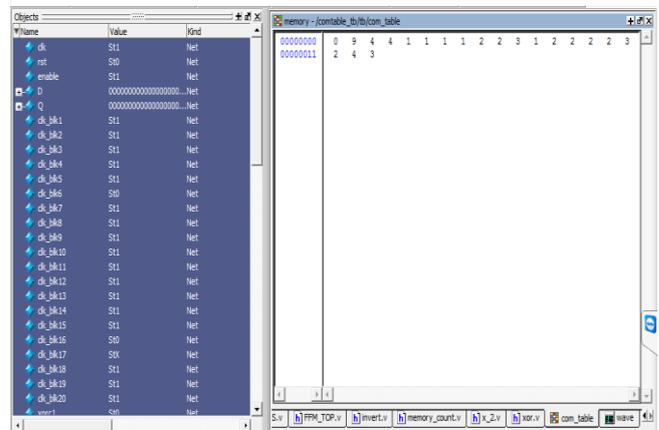

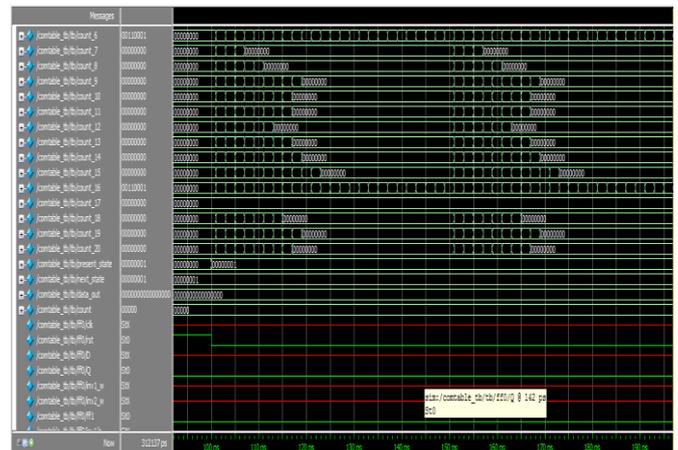Figure 9: Merging flip-flop count

Figure 10: Flip-Flop merging output

The flip-flops are merged based on the clock synchronization. Initially, we identify the flip-flops which are having same clock phase signal. Then those flip-flops are merged to reduce the number of inverters and hence the clock power is reduced. Due to the reduction in number of inverters, total area also reduced. The table I shows the power consumed by the flip-flops in different Stages. After flip-flop merging, some flip-flops are in ideal stages. Those flip-flops are also consumes the power.

TABLE I. POWER ANALYSIS

Parameters	Power (mW)
Before Merging	539.25
After Merging	105.12
Clock Gating	72.93

Clock gating is used to block the clock signal which is consumed by the ideal flip-flops. Hence the power consumption is further reduced

IV. CONCLUSION

In this paper, the flip-flops are merged based on the combination table. The process of identifying the mergeable flip-flops and building a combination table, in which the possible combinations of flip-flops are merged, are executed. This multi-bit flip-flops will reduce the unnecessary power wastage and total area of the digital circuits. Additional contribution of this paper is the number of flip-flops to be merged is increased using pulse width modulation by adjusting the width of the clock pulse.

V. REFERENCES

[1] Y. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and Q. Wang, "Power-aware placement," in proc. Design Autom. Conf., pp. 795-800, Jun 2005.

[2] Y.-T. Chang, C.-C. Hsu, P.-H. Lin, Y.-W. Tsai, and S.-F. Chen, "Post-placement power optimization with multi-bit flip-flops," in proc. IEEE/ACM Compt.-Aided Design Int. Conf., San Jose, CA, pp. 218-223, Nov. 2010.

[3] J.T. Yan, Z.W. Chen, "Construction of constrained multi-bit flip-flops for clock power reduction," in Green Circuits and Systems Int. Conf., pp. 675-678, 2010.

[4] Zhi-Wei Chen, Jin-Tai Yan, "Utilization of Multi-Bit Flip-Flops for Clock Power Reduction,"IEEE Conference on Circuits and Systems, pp.677-680,2012.

[5] P. Gronowski, W. J. Bowhill, R. P. Preston, M. K. Gowan, and R. L. Allmon, "High-performance microprocessor design," IEEE Solid-State Circuits, vol.33, no. 5, pp. 676–686, May 1998.

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