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SEMICONDUCTOR DEVICE TESTING

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Abstract— **Before shipping the wafers or components back to the customers or to the supply chain they must be verified that no damage on the material to test the wafer you need a wafer prober automatic test equipment a probe card and a customized test program after loading the test program the wafer lot is placed in the wafer prober and programmatically selects one wafer at a time for testing the wafer. With the vacuum an advanced positioning system helps to move the chunk around in a rapid and very accurate pattern below the probe card in order to test every single device on the wafer and the tester generates a wafer map which shows which devices are good and which are bad this information is used later in the supply chain when the wafers are being further processed wafers intended for encapsulation are sent to partners after encapsulation they are returned for component testing to test components. For that process you need a component handler automatic test equipment a customized load board and a customized test program once the test program loaded the components are placed in handler the handler ensures that the device under test is moved to the correct position on load board the output of test is a separation of good and bad components in order to protect wafers and components from humidity and electrostatic discharge they are sealed under vacuum in anti-static bags after testing the wafers or components they are inspected once more before packaging and shipping to the customer.**

Index Terms—**About four key words or phrases in alphabetical order, separated by commas.**

I. Environmental conditions for semiconductor testing:

The environment in which the airborne particles are controlled by specified limits this is done by controlling air flow rates and pressurization temperature and humidity.

Anti-static lab coats and shoes are to be used before operators enter and they must ground themselves connecting the anti-static wrist straps thus removing static charges that might damage the semiconductor devices.

The silicon wafers or components are stored according to quality standard all wafers must be in particle free nitrogen cabins where the temperature and relative humidity are constantly controlled.

II. About ATE:

ATE is an assortment of test instruments constrained by an elite PC.

- It is utilized to test coordinated circuits by executing test programs
- ATE is a test framework comprising of DC, Analog, Digital kinds of hardware constrained by a test PC to do designing/characterization tests on IC'S
- Several utilitarian tests dependent on many voltages, current and timing tests are required to guarantee the total usefulness of the DUT. To play out these perplexing testing consequently, ATE is required
- ATE delivers exceptionally steady test outcomes rapidly and dependably without bargaining the exactness of the test.
- a similar analyzer can be utilized to test a wide assortment of gadgets, diminishing the general effect of the capital venture required to use an analyzer.
- Help in accomplishing a shorter "Time to Market".

III. Testing:

Testing is the process of categorizing the detective from non-defective, creating a catalogue for good and bad devices.

It ensures and guarantee the quality product to meet the device specifications, to characterize the device performance/working and provide the feedback for the design of device. It identifies the failures, faults and errors at starting phase to save cost.

IV. Project plan:

Project plan is the documentation of goals, procedures, possibilities, expected outcomes, timing information etc., with all the data or information available for the device. To characterize scope, prerequisites, plan, assets, cost, objective, course of events, anticipated execution and certainty level. To quantify the advancement of testing exercises by looking at actual execution/performance against anticipated execution.

a) Advantages of project plan:

- Communication among individuals
- Risk management
- Overcome the chances of faults, failures, errors when the test is executing.
- To identify the process

The majority of the expenses are related with testing without the vision what to be done/accomplished and how it is to be done testing cost will not reduce.

b) Prerequisites for Project plan:

- **DUT Prerequisites**
  1. Description of each pin

2. DC & AC specifications of the device
3. Signals Requirements for input/output
4. Details of parameters to be tested
5. Specifications of tests and tests to be executed are to be included.
6. The hardware setup for testing (load board) should be prepared accordingly.
7. Based on the test plan the test program should be generated.

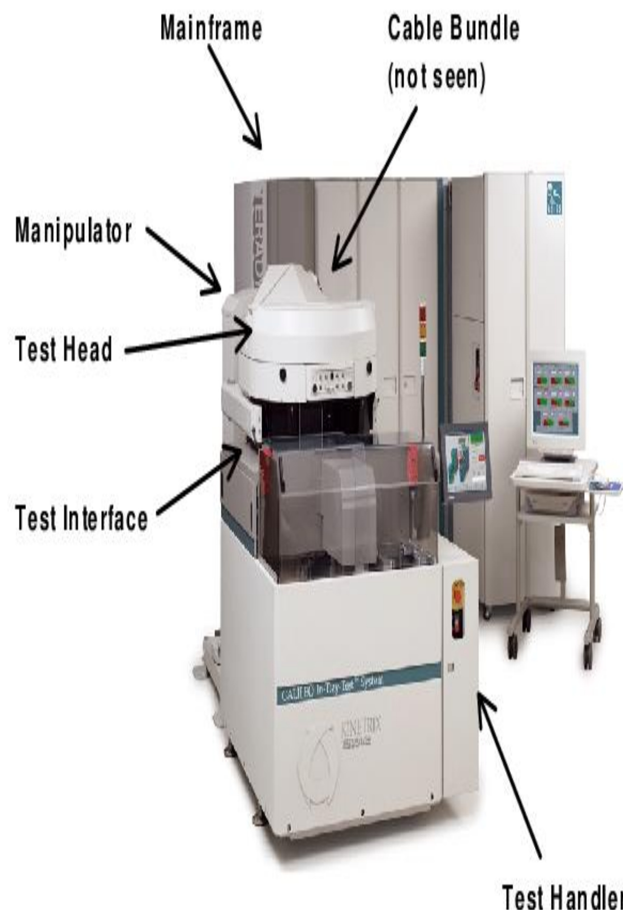
- **Software:**
  1. Software to generate and run the test program
  2. At the end, the test results are recorded and the binning result sent to the operator
- **About tester:**
  1. Availability of instruments
  2. Programmability of instrument
  3. Specification manual
  4. Accuracy of instruments
- **Device interface:**
  1. The purpose is to connect the DUT pins to the system to send and receive signals.
  2. DIB is the hardware interface between the DUT and the tester.

V. TEST PROGRAMS:

- **Program for production test:** The test program should be fast for Wafer sort, final test, quality assurance test should be done and the faults and failure devices are to be segregated to find out the yield.
- **Program for characterization test:** It is the augmentation of program for engineering test, to decide the possible operating values and limits. Tester pre-characterized schedules ought to be utilized to plot the portrayal diagram for Shmoo, level pursuit and time search routines. Characterization program is utilized to totally check the device meets its particular and gathering portrayal information.
- **Program for engineering test:** The starting test program for testing functionality of the device is test program for engineering. It is flexible for altering currents, timings and voltages and quick troubleshooting and some portrayal schedules ought to be accessible.
- **Considerations**: The availability of system, throughput, yield, limitations of hardware and software, DUT cost and test cost should be considered. For creating the test program resources of tester, design of load board is also to be considered.

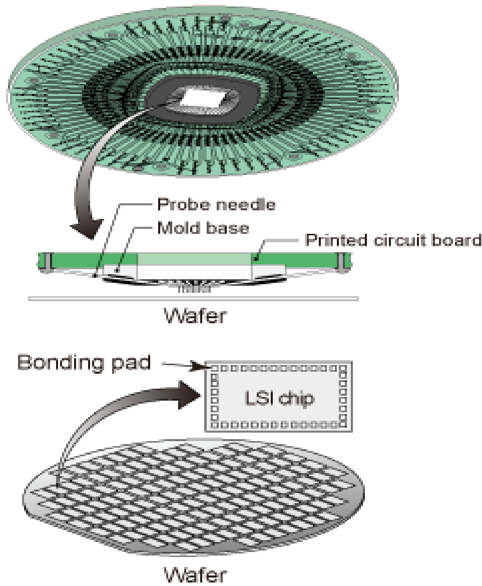
VI. COMPONENTS IN TEST SYSTEM:

6.1 Load board or Test interface board: A load board additionally known by different names including test interface unit and execution board is an interface between the IC under test and the test head of the parametric analyzer or automated test hardware (ATE). A load board, as a rule, comprises of a test attachment or a socket that holds an IC and mounts to a printed circuit board (PCB), otherwise called a DUT or ATE board, which mounts to the test head of an ATE. The load board gives a basically straightforward mechanical and electrical interface between the IC and the ATE. This permits precise, accurate and reliable verification of IC circuit uprightness and execution.



6.2 Probe card: A probe card is utilized for electrical testing of a chip on a wafer during the wafer test process and manufacturing. A probe card is docked to a wafer prober to fill in as a connector between the chip and analyzer as an estimating machine (ATE). The needles of the probe card contact the chip terminals to lead electrical testing

for the go/off-limits test. The wafer test process is profoundly significant and exceptionally subject to the unwavering quality of probe cards**.**



6.3 Handlers: ATE frameworks normally interface with a mechanized position device, called a "handler", that genuinely puts the Device Under Test (DUT) on an Interface Test Adapter (ITA) so it very well may be estimated by the gear. There may likewise be an Interface Test Adapter (ITA), a gadget simply making electronic associations between the ATE and the Device Under Test (additionally called Unit Under Test or UUT), yet additionally, it may contain extra hardware to adjust flags between the ATE and the DUT and has physical offices to mount the DUT. At long last, an attachment is utilized to connect the association between the ITA and the DUT. An attachment must endure the thorough requests of a creation floor, so they are normally supplanted as often as possible. Basic electrical interface chart: ATE → ITA → DUT (bundle) ← Handler.

6.4 Manipulator: Manipulators are good with all significant wafer prober or gadget handler models and can oblige test goes to 500 kg (1,100 lb.). Broad analyzer similarity ,Broad prober and handler similarity , Excellent opportunity for movement , Simple to utilize.

6.5 Prober: A wafer prober is a framework utilized for electrical testing of wafers in the semiconductor improvement and assembling process. In an electrical test, test signals from an estimating instrument or analyzer are transmitted to singular gadgets on a wafer by means of test needles or a test card and the signs are then come back from the gadget. A wafer prober is utilized for taking care of the wafer to reach in the assigned situation device.

VII. CONCLUSION:

The development and debugging of the device for functionality test and other Parametric tests can be done Easily and there are many other components to be added test the device and there are many ways to program and to test but the aim is to reduce the time for testing.

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