International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)
ISSN: 0976-1353 Volume 24 Issue 10 – JULY 2017.

Irradiation Experiments on SRAM-FPGAs and its Test Setups: An Overview

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***Abstract*— Design of Instrumentation and control systems in terrestrial and spatial applications face radiation effects as the major challenge. The radiation effects in electronic devices can be classified as total ionisation dose (TID) effects, displacement damage dose (DDD) and single event effects (SEE). SRAM-based FPGAs are becoming more popular in safety critical and safety-related application development. But the major threat to these FPGAs in safety critical applications is the vulnerability to radiation effects. Most of the radiation effects in terrestrial applications are recoverable ie, the errors are temporary in nature and the affected system can be reset to its original state. The faults which are non-recoverable generate permanent damage in the system. In safety critical applications even if the system fails it should fail in a fail-safe mode so for this purpose the sensitivity of the device in radiation environment need to be known. Irradiation experiments are necessary to measure the sensitivity of the FPGAs. This paper reviews the irradiation experiments performed on SRAM-based FPGAs at various facilities with the various experimental test setups and methodologies.**

***Index Terms*—FPGAs, Irradiation Experiments, Radiation Effects, Single Event Upset, Total Ionization Dose**

I. INTRODUCTION

SRAM-based FPGAs are following the CMOS process technology so the feature size is decreased drastically compared to flash and antifuse FPGAs. This advancement in process technology increases the logic density and reduces the core voltage; due to this the device is susceptible to radiation effects. The major effects of radiation on electronic devices are total ionisation dose (TID) effects, displacement damage dose (DDD) and single event effects (SEE) [1]. TID effects are due to the cumulative dose absorbed by the device during its whole life, DDD is caused due to the change in the lattice structure of the device material by energetic particle strike and SEE is caused by a single energetic particle strike [2].

TID can cause threshold voltage shift, increase in leakage currents and change in transconductance values of MOS transistors. The charge deposition in Si/SiO2 layer can also cause SEEs in the device. The damage caused by TID effects can be either temporary or permanent [3-5]. DDD effects damage the device permanently as it alters the position of atoms from its lattice structure [6-7]. SEEs can be classified as hard errors or non-recoverable errors and soft errors or recoverable errors [8]. Hard errors are categorized as single event latchup (SEL), single event burnout (SEB) and single event gate rupture (SEGR) etc [9-11]. Soft errors are categorized as single event upsets (SEU), single event transients (SET) and single event functional interrupt (SEFI) etc [12-15].

SRAM-based FPGAs constitutes configuration layer and the user layer. The configuration layer constitutes the configuration memory, configuration access ports and the control circuitry [16]. The user layer consists of user logics, input/output blocks (IOB), and user memory (Block RAMs and distributed RAMs) etc. The configuration memory holds the functionality of the system implemented and the information on routing. User memory holds the value of the current state of the system [17]. Before deployment of the system in radiation environment the device needs to be checked for its radiation tolerance level. Based on the sensitivity of the device, various fault tolerant mechanisms can be implemented to prevent the failure of the system [18]. In the terrestrial environment the major cause for reliable applications are SEUs and TIDs, so the major objectives of irradiation testing on SRAM-FPGAs are listed as [19]:

a. SEU sensitivity of configuration memory and Block RAM cells (With and without mitigation techniques).
b. SEU Sensitivity of Input / Output Blocks (IOBs).
c. Measure SEFI modes (Power On Reset (POR), SelectMAP, IOB, etc.)
d. Measure the Total Ionization Dose (TID) effects.

This paper is organized based on the irradiation experiments carried out in various laboratories worldwide. This gives an overview of the irradiation experimental test setups, the method of experiments and the results of irradiation tests. This would be helpful to the researchers and design engineers who work on the system reliability which needs to be deployed in a radiation environment.

II. IRRADIATION EXPERIMENTS

A. Test Case 1

The testing conducted at the Texas A&M University Cyclotron Institute on the DUT Virtex reprogrammable FPGA (XQVR300) from Xilinx mainly for verifying the SEL immunity above 100 MeV-cm2/mg. Detailed SEU testing was conducted in both static and dynamic operating conditions to better understand the upset modes and develop mitigation techniques [20].

The test algorithm was implemented as follows: 1) Write configuration bit stream with "all-off" data pattern. 2) Verify correct configuration with readback. 3) Note quiescent current consumption. 4) Pause while ion beam is applied to a given fluence. 5) Note current consumption. 6) Verify post radiation configuration with readback. 7) Compare data before and after radiation. 8) Record bit upsets for all logic blocks. 9) Configure & readback, verify current returns to quiescent level and configuration/readback function as expected. 10) Repeat at various LET and fluence values and plot SEU characteristic [20].

The device was initialized with "all off" pattern and exposed to Au ions to achieve an effective LET of 125 MeV-cm2/mg at 2,068 MeV with an incident angle of 30°, and the dose was allowed to accumulate to 107 ions/cm2 for most runs and in one case it is 108 ions/ cm2. The power supply was set to 2.5volts and the current in each test is monitored. The current measured initially is 10 to 20 mA and it has increased to 300 to 500 mA at the end of the exposure. After reconfiguration, the measured current is same as the initial value so the part is not latch-up to a LET of 125 MeV-cm2/mg. The current increase was due to internal contention created by logic upsets accumulating throughout each run. At 108 ions/cm2 an increase in current that remained after reconfiguration and power cycling. This was attributed to the equivalent ionizing dose (>100 Krad (Si)) accumulated by such a large fluence; the device annealed over a few hours. Despite the dose induced parametric degradation, the device remained functional. The SEU characteristics of latch types are given in Table I [20].

Table I SEU Characteristics of Latch types

Latch Type	Threshold LET (MeV-cm^2/ mg)	Saturation Cross section (cm^2)
CLB	5	6.5×10^8
LUT	1.8	21×10^8
BRAM	1.2	16×10^8
Routing bits	1.2	8×10^8

B. *Test Case 2*

The evaluation of SEUs is performed based on a combination of irradiation test and simulation based fault-injection is explained in [21]. The device under test (DUT) is Xilinx Virtex XQVR300 FPGA and the test is performed by a power PC-based (MPC860) microprocessor system and the control circuitry implemented in another Virtex FPGA. The experimental setup block diagram is shown in fig. 1.

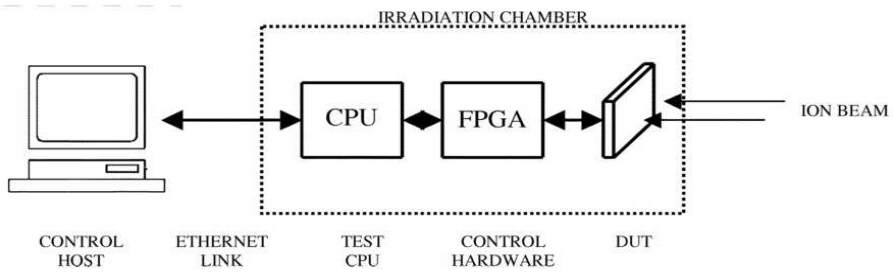

Fig. 1. Experimental setup. The control host is about 50 m away from the irradiation chamber that contains the power PC-based microprocessor system (CPU), the control hardware (FPGA), and the DUT, all located within a distance of 10 cm.[21].

Three different test algorithms are used in this experiment. In the first one, the DUT without any stimulus is irradiated with various types of ions with different intensities to find out the SEU rate and subsequently compute the device cross-section per bit for every resource type. The control hardware periodically does the configuration readback and detects the number of SEUs generated. The second test algorithm is meant for SEFI cross section measurement. The configured device is exposed to the beam and continuously stimulated and monitored from the control hardware. While analysing the occurrence of SEFI in these tests it is difficult to say that which SEUs cause the SEFI. So a third test algorithm is proposed as similar as the second one, but in this case, the DUT is periodically reconfigured. The length of the reconfiguration period is selected in such a way that on an average one or two SEUs could occur before the DUT is reconfigured. Each of these algorithms was applied to the test circuit in sequence for each ion. The beam flux is adjusted in such a way to obtain more than one SEUs and not less than 0.2 SEUs. The heavier the ion, the larger the cross section and, consequently, the corresponding SEU probability. The beam flux was set between 20 ions / (cm^2. s) for ions with LET > 10 MeV. cm^2 /mg and up to 15000 ions / (cm^2. s) for the others. Based on these experiments it's concluded that the LUT bits are the most sensitive to SEUs. For conducting experiment different user circuits were implemented and it is found that the device cross section does not depend on the specific circuit [21].

The experimental measurements were normalized to the total number of configuration bits, and they were fitted by using the Weibull formula. The device cross section formula is given in Equation 1.

$$DCS\,(LET) = DCSsat \cdot \left[1 - e^{-\left[\frac{LET - LET_0}{W}\right]^s}\right] \qquad (1)$$

Where, DCS per bit is measured in cm^2/bit from the experimental results, it is calculated as $DCS_{sat} = 2.2 \times 10^{-8}$ cm^2/bit, is the saturation level, and $LET_o = 0.9$ MeV.cm^2/mg is the threshold level, w = 8.5 and s= 3.2 are fit parameters of the Weibull plot. The saturation level found in these experiments is similar to that reported in [21] for a Virtex XQVR300 Xilinx FPGA.

In Table II, the ratio between the configuration SEU cross section and the SEFI cross section has been calculated for each ion. This ratio corresponds to the number of errors in the configuration memory needed to induce an SEFI in the user circuit.

B14 and C_6288 are two different designs that run during irradiation (20% of total FPGA resources for B14 and 60% for C_6288). The SEFI cross section for the C-6288 circuit is higher than for B14, due to both different area occupations of the two circuits and different architectures. From Table II it is

observed that the decreasing of SEU/SEFI ratio with the LET increasing [21].

By using the third experimental procedure where each read-back bitstream contains only one erroneous bit, and where the erroneous bit is responsible for an SEFI in the implemented circuit, i.e., the C_6288 circuit. All of these bitstreams have been examined, and the faulty bits have been classified as previously described. Obtained results are summarized in Table III.

Table II. SEU/SEFI Ratio

Ion	LET (MeV/mg/cm^2)	B14 SEU/SEFI	C_6288 SEU/SEFI
^{12}C	1.6	296	33
^{16}O	3	783	12
^{19}F	4.1	101	8
^{28}Si	8.5	36	6
^{35}Cl	12.5	42	
^{58}Ni	30	51	9
^{107}Ag	58	11	
^{127}I	64	37	

Table III. SEU Effects on FPGA Resources

Type of FPGA Resource	Type of SEU Effect	SEU Effect Total events	SEU Effect Frequency [%]
PIPs	Open	57	13
PIPs	Antenna	6	1.5
PIPs	Short	105	24
Other	Other	267	61.5

Through experimental tests, it is demonstrated that the configuration memory of Xilinx Virtex XQVR300 FPGA is highly sensitive to heavy-ion-induced SEUs, and particularly, the LUT elements are the most sensitive parts.

C. *Test Case 3*

The test is composed of three components, the DUT, the configuration monitor and the functional monitor. The DUT is Xilinx XCV100 Virtex FPGA situated on Xilinx AFXBG256-200 development board.

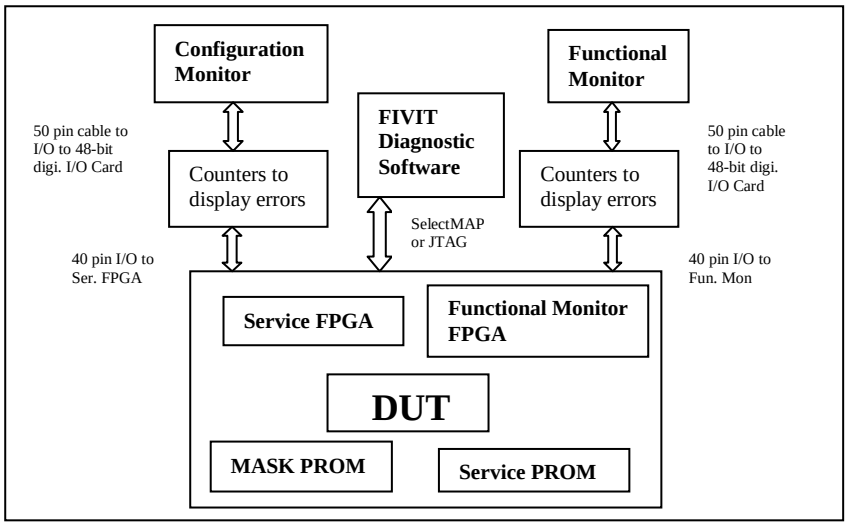

Figure 2. Experimental setup at Crocker Nuclear Laboratory [22].

Another XCV100 is used as configuration monitor as also known as the service FPGA used to detect and correct configuration upsets with the help of a host computer [22]. A Spartan XCS30XL FPGA is used as a functional monitor to generate the test vectors to verify the functionality. The test setup is illustrated in figure 2. The configuration readback data is compared bit-for-bit of the mask file stored in the "Mask PROM". If there is any mismatch the configuration monitor FPGA sends a signal to the host computer, the custom visual basic program records and displays the errors as they occur [22]. When an error is detected the service FPGA corrects the error by partial reconfiguration (PRC) without disturbing the operation of the design implemented, also called as non-intrusive-scrubbing [23]. The results of test cases compared with the DUT outputs are also sent to the second host computer and it is recorded and displayed. The experiment facility, source used and device cross section are given in Table IV.

Table IV. Experimental Results

Source	Heavy-ion	Energy range	LET Range	Flux range	Cross section
Degrading the 10.7 MeV cyclotron energy by 72.6 µm (3 mils) Ta foil.	Proton	6.8 MeV	1.5 – 63 MeV cm^2 / mg	10^4 -10^9 p/ cm^2.s^{-1}	1×10^{-7} - 1×10^{-8} cm^2/ device

D. *Test Case 4*

The objective of the test conducted at TRUMF Proton Irradiation Facility (PIF), University of British Columbia, Canada is to establish the upset cross section of certain functional blocks of the Spartan 6 XC6SLX45T, to investigate the possible latchup sensitivity and to establish the total dose (protons) performance [24]. Two beam lines available in the facility are with 180-520 MeV energy with intensity 105 - 4×107 proton/cm2/s and 65-120 MeV energy with intensity 105 - 108 proton/cm2/s respectively. The SEU test setup block diagram is illustrated in figure 3. To evaluate SEU performance two types of tests were performed.

First one followed the static test procedure i.e., configured the device with a known pattern without any clock applied and irradiated the device. At the end of the SRAM was read back via the JTAG interface using iMPACT console [24], the number of upsets detected and the fluence is recorded and the device is reconfigured with the known pattern. This test evaluated the SEU cross section of the SRAM which stores

the logic configuration. The device's power rails were monitored remotely in a laptop computer using a current probe connected to the network capable oscilloscope. This test is named Spartan-6 SRAM Logic Configuration.

The outputs of self-checks from the device under test (DUT) were connected to a second identical monitoring platform (MON) via a high-density ribbon cable.

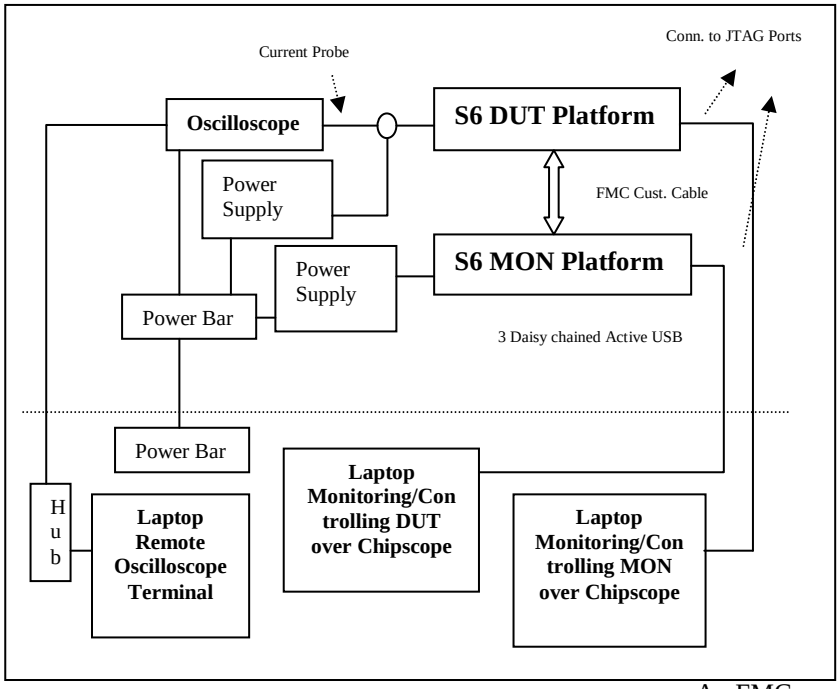

Fig. 3. The SEU Test Setup TRUMF Proton Irradiation Facility [24]

In the second type, the dynamic test procedures are followed to evaluate the SEU performance of certain functional blocks of the device: CLBs and FFs, multipliers, and BRAM. These tests are named Spartan-6 CLBs and FFs, Spartan-6 Multipliers, and Spartan-6 BRAM, respectively. These tests do not distinguish between upsets in the SRAM storing the logic configuration and user logic. The test designs included monitoring and self-checking features which allowed SEUs to be monitored during irradiation.

An FMC connection port was used for that purpose which is included in the Spartan-6 FPGA SP605 Evaluation Platform (EP) [25] for CLBs, FFs, BRAM and multipliers. Xilinx ChipScope [26] was implemented on MON and used to monitor the outputs. The number of errors accumulated during irradiation in the SRAM storing the logic configuration was also monitored. Whenever an SEU was detected by the MON the beam was halted, fluence to upset, a number of errors observed, upset signature, number of bit flips in SRAM storing logic configuration, and recovery method was recorded.

The cross section configuration memory, CLBs, multipliers and BRAM are given in Table V. The fluence and the number of upsets on Spartan 6 resources are given in Table VI

Table V. Cross sectional values of FPGA resources

	Spartan 6 XC6SLX45T [27]	**Virtex 6 XC6VLX240T** [28]	**Virtex-5 XC5VLX50T** [28]	**Virtex-4 XC4VLX25** [29]	**Virtex-II XC2V1000** [30, 31]
SRAM storing logic Configuration	8.1×10^{-15} cm^2/bit	9.7×10^{-15} cm^2/bit	19.5×10^{-15} cm^2/bit	15.6×10^{-15} cm^2/bit	33.6×10^{-15} cm^2/bit
CLBs and FFs	16.4×10^{-15} cm^2/FF	7.4×10^{-15} cm^2/FF	24×10^{-15} cm^2/FF	66×10^{-15} cm^2/FF	88×10^{-15} cm^2/FF
Multipliers	3.2×10^{-12} cm^2/Multiplier	5.4×10^{-12} cm^2/Multiplier	10×10^{-12} cm^2/Multiplier	10×10^{-12} cm^2/Multiplier	78×10^{-12} cm^2/Multiplier
BRAM	14.1×10^{-15} cm^2/bit	1.7×10^{-15} cm^2/bit	2.4×10^{-15} cm^2/bit	4.2×10^{-15} cm^2/bit	4.7×10^{-15} cm^2/bit

Table VI. Upsets generated in Spartan 6 FPGA Resources

Spartan 6 FPGA Resources	**Fluence (p/cm^2)**	**Number of Upsets**
SRAM storing logic configuration	1.03×10^9	121
CLBs & FFs	19.3×10^9	1961 bit flips
Multipliers	9.44×10^9	1575 bit flips
BRAM	651×10^6	83-bit flips

E. Test Case 5

The experiment conducted at Heavy Ion Research Facility in Lanzhou (HIRFL) on Virtex-II- XC2V1000-4bg575i device with Kr-86 ions have studied the relationship between dynamic current and the quantity of SEUs in the configuration memory. The current increases with increase in SEUs it happens probably due to the routing resources confliction resulting from SEUs in the configuration memory [32]. The ion beam parameters are given in Table VII.

Table VII. List of Ion beam parameters

Energy (MeV)	LET (MeV/mg/cm^2)	Range (Si) (µm)	Flux (Ions/cm^2/s)
1493	23.57	207.5	30/100/600

JTAG interface is used to readback the configuration memory content of XC2V1000 as well as configuring. By comparing the readback data to the configuration file the number of SEUs can be counted. The workload applying for the test is a TMR structure signal generator module based on a direct digital synthesis (DDS). A module named logic probe is applied to detect routing error indirectly. The test setup used is shown in figure 4 [32].

Table VIII. Current variation and SEU rate at various flux range

DUT: Virtex-II- XC2V1000-4bg575i; Facility: Heavy Ion Research Facility in Lanzhou (HIRFL); Heavy Ion Used: Kr-86			
Flux range (ions/cm^2/s)	Time of irradiation (Seconds)	Current variation (Ampere)	SEU rate (upset/ions)
30	139	0.54 – 0.61	0.82
30	304	0.54 – 0.57	0.82
100	540	0.54 – 0.69	0.61
100	124	0.54 – 0.57	0.72
300	69	0.54 – 0.63	080
300	2589	0.54 – 1.14	0.33
600	2882	1.10 – 2.60	0.3

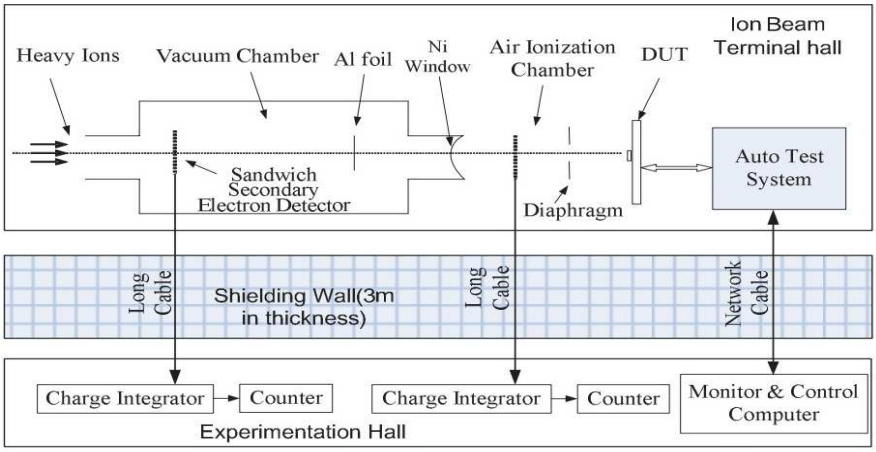

Figure 4. Schematic of the Test Facility for applying Kr 86

There is no sudden and persistent increase of current is observed during the experiment and it is considered as an important attribute for Single Event Latchup (SEL). During irradiation current increases and after reconfiguration the current drops to the initial value 0.54A. In most cases, current increases with more SEUs and it also drops when more SEUs occurred. The experimental data is given in Table VIII [32].

F. Test Case 6

In the whole-chip irradiation experiment, TID analysis of SRAM-based FPGA is implemented using on-line test system and IC parameter analyzer. The corresponding TID failure modes can be summarized as the inability to be reconfigured and to be powered up. In the synchrotron X-ray irradiation experiment, a functional error resulting from the failure of Power-on Reset (POR) component is observed, which prove that the specified zone in POR circuit is very sensitive to TID, and the failure of POR circuit could be related to the failure mode inability to be powered up. The schematic picture of synchrotron X-ray irradiation environment is shown in figure 5 [33].

The whole-chip TID experiment is executed using Co-60 source in Northwest Institute of Nuclear Techniques, the dose rate equals to 50rad (SiO2)/s. Before the irradiation experiment, the SRAM-based FPGA was configured with a specified design, containing two shift registers (with 9-bit width and 5440-bit depth) and two FIFOs (with 16-bit width and 2048 depth).

All together, 98% of the available CLB D-FFs resources and 100% of the available block RAMs in the device have been used. During the irradiation procedure, the SRAM-based FPGA would operate in static mode (the clock input is high) or dynamic mode (the clock speed is chosen to be 20MHz). The measurements of supply currents are performed continually. To check for the possible data errors occurring in configurable RAM and block RAM, the bitstream file is read back and verified every 5 seconds. After the deposited dose is bigger than 50krad(SiO2), the reconfiguration is performed every 5krad(SiO2) to inspect possible functional error. In addition, before and after the irradiation, electrical parameters of DUTs are measured with IC parameters tester [33].

In the static operating mode, when the deposited dose arrives at 75 krad (SiO_2), the DUT can't be reconfigured any more. Till the deposited dose reaches 60 krad (SiO_2), and no functional error occurs.

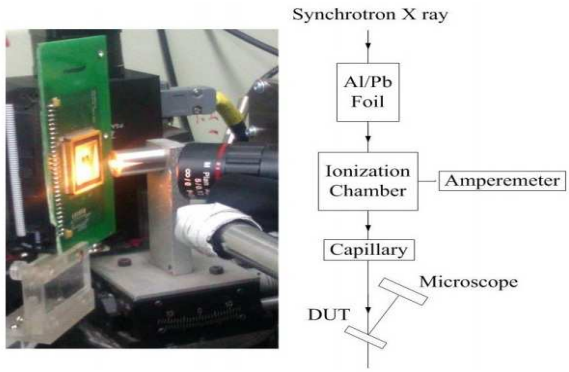

Figure 5. Schematic picture of synchrotron X-ray irradiation environment

In dynamic mode of testing the supply current would be much higher than in the static mode. The supply current variation in static biased and dynamic biased are shown in figure 6 and 7 respectively. DUTs work functionally till 65krad (SiO_2), but can't be reconfigured when the deposited dose arrives at 70krad (SiO_2). During the irradiation procedure, the failure modes can be summarized as follows. Firstly, the supply currents for devices and I/O logic (not presented in the above figures) keep increasing with deposited dose, but this trend becomes visible only when the value of deposited dose is big enough (>60krad(SiO_2)). Secondly, inability to be reconfigured is one of the most severe functional errors for devices irradiated in static mode and dynamic mode (70-75 krad (SiO_2)). Thirdly, inability to be powered up is the failure mode with the lowest failure threshold dose (60krad (SiO_2)) [33].

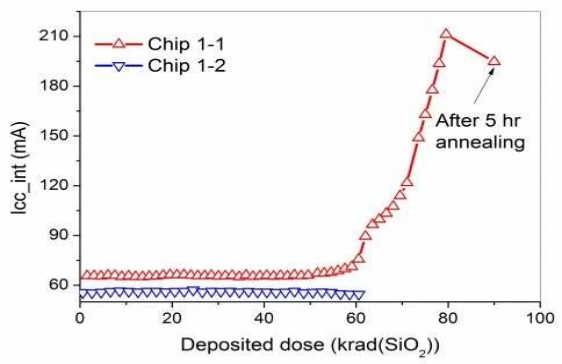

Figure 6. Supply current of DUTs (I_{CC}) as a function with deposited dose when the DUTs are biased in static mode during the irradiation procedure.

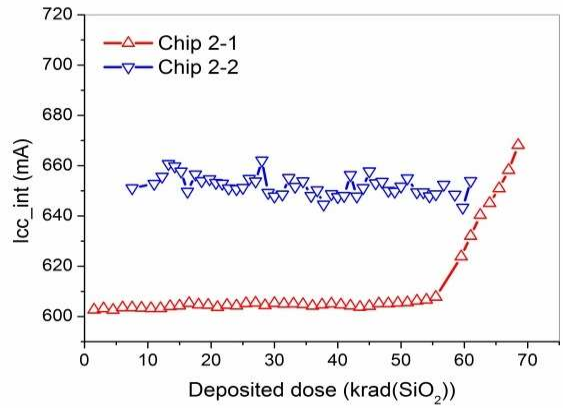

Figure 7. Supply current of DUTs (I_{CC}) as a function with deposited dose when the DUTs are biased in dynamic mode during the irradiation procedure.

III. CONCLUSION

The importance of irradiation experiments is to measure the sensitivity of the devices in a radiation environment, to measure the life of the device being functional and also to predict the failure of the system implemented in the device. The major radiation effects in terrestrial application developments are single event upsets and total ionization dose effects. The method commonly used in the experiments for measuring SEU sensitivity is by measuring the cross section/bit. This is performed by reading back the configuration memory and comparing with the golden readback file at particular particle fluence. TID measurements are performed based on the increase in power supply current, propagation delay and the inability to reconfigure the device.

ACKNOWLEDGMENT

The first author gratefully acknowledges the grant of the research fellowship from the Department of Atomic Energy, Government of India.

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