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Design and Implementation of BIST for ISCAS-85 C432 Combinational Circuit

Chintalapudi Srikanth Tataji[*1], and CH.Kanakalingeswararao[#2]

[*]*Student, Dept of Embedded Systems, Jogaiah Institute of Technology and Sciences College of Engineering, India*

[#]*Asst. Professor, Dept of Embedded Systems, Jogaiah Institute of Technology and Sciences College of Engineering, India*

[1]srikanthtataji.mtech@gmail.com

[2]klr_mani786@yahoo.co.in

***Abstract*— In this proposed method we are test the one combinational circuit. Here this combinational circuit having 36-bit input and 7-bit output. ISCAS-85 C432 27-channel interrupt controller is a combinational benchmark circuit. This paper described an on-chip test generation method for functional broadside tests. The hardware was based on the application of primary input sequences initial from a known reachable state, thus using the circuit to produce additional reachable states. Random primary input sequences were changed to avoid repeated synchronization and thus yield varied sets of reachable states. The hardware structure was simple and fixed, and it was tailored to a given circuit only through the following parameters: the length of the LFSR used for producing a random primary input sequence; the length of the primary input sequence; the specific gates used for modifying the random primary input sequence; the particular gate used for selecting applied tests; and the seeds for the LFSR. With the proposed on-chip test generation method, the circuit is used for generate reachable states for the duration of test application. This alleviates the want to compute reachable states offline.**

Index Terms—Built-in test generation, functional broadside tests, ROM, reachable states, transition faults, test pattern generator, ISCAS-85 C432 benchmark circuit.

I. INTRODUCTION

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT), as illustrated in Figure 1. The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a check controller. The test pattern generator generates the test patterns for the CUT. Example of pattern generators are a ROM with stored patterns, counter and a linear feedback shift register (LFSR). A typical reply analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It a compacts and analyzes the test responses to conclude exactness of CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, some test-related functions can be executed through a test controller circuit.

As shown in Figure 1, the wires from primary inputs (PIs) to MUX and wires from circuit output to primary outputs (POs) cannot be tested by BIST. In regular operation, the CUT receive its inputs from other modules and performs the function for which it was designed. During test mode, a test pattern generator circuit applies a sequence of test patterns to the CUT and the test response are evaluated by a output response compactor. In the most common type of BIST, test responses are compacted in output response compactor to form (fault) signatures. The response signatures are compare with reference golden signatures generated or stored on-chip, and the error signal indicates whether chip is good or faulty.

Four primary parameters must be considered in developing a BIST methodology for embedded systems; these correspond with the design parameters for on-line testing techniques discussed.

- Fault coverage: This is the fraction of faults of interest that can be exposed by the test patterns produced by pattern generator and detected by output response monitor. In presence of input bit stream errors there is a chance that the computed signature matches the golden signature, and the circuit is reported as fault free. This undesirable property is called masking or aliasing.
- Test set size: This is the number of test patterns produced by the test generator, and is closely linked to fault coverage: generally, large test sets imply high fault coverage.
- Hardware overhead: The extra hardware required for BIST is considered to be overhead. In most embedded systems, high hardware overhead is not acceptable.
- Performance overhead: This refers to the impact of BIST hardware on normal circuit performance such as its worst-case (critical) path delays. Overhead of this type is sometimes more important than hardware overhead.

II. BLOCK DIAGRAM OF BIST

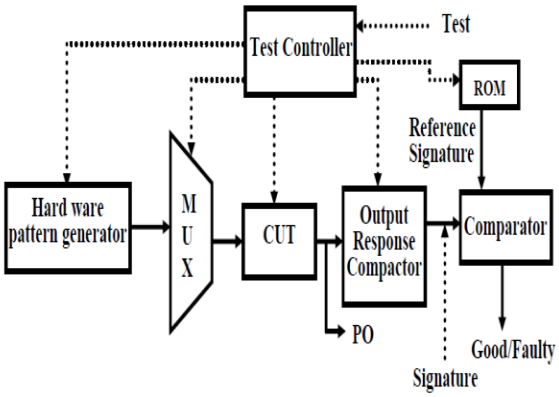


Figure 1 Block diagram of BIST

BIST can be used for non-concurrent, on-line testing of the logic and memory parts of a system [2]. It can readily be configured for event-triggered testing, in which case, the BIST control can be tied to the system reset so that testing occurs during system start-up or shut down. BIST can also be designed for periodic testing with low fault latency. This requires incorporating a testing process into the CUT that guarantees the detection of all target faults within a fixed time.

On-line BIST is usually implemented with the twin goals of complete fault coverage and low fault latency. Hence, the test generation (TG) and response monitor (RM) are generally designed to guarantee coverage of specific fault models, minimum hardware overhead, and reasonable set size. These goals are met by different techniques in different parts of the system.

TG and RM are often implemented by easy, counter-like circuits, especially linear-feedback shift registers (LFSRs). The LFSR is simply a shift register formed from standard flip-flops, with the outputs of selected flip-flops being fed back to the shift register's inputs. When used as a TG, an LFSR is set to cycle rapidly through a large number of its states. These states, whose choice and order depend on the design parameters of the LFSR, define the test patterns. In this mode of operation, an LFSR is seen as a source of (pseudo) random tests that are, in principle, applicable to any fault and circuit types. An LFSR can also serve as an RM by counting (in a special sense) the responses produced by the tests. An LFSR RM's final contents after applying a sequence of test responses forms a fault signature, which can be compared to a known or generated good signature, to observe if a fault is present. Ensuring that the fault coverage is sufficiently high and the number of tests is sufficiently low are the main problems through random BIST method. Two general approaches have been proposed to preserve the cost advantages of LFSRs while making the generated test sequence much shorter. Test points can be inserted in the CUT to improve controllability and observability; however, they can also result in performance loss. Alternatively, some determinism can be introduced into the generated test sequence, for example, by inserting specific "seed" tests that are known to detect hard faults.

A typical BIST architecture using LFSR is shown in Figure 2. Since the output patterns of the LFSR are time-shifted and repeated, they become correlated; this reduces the effectiveness of the fault detection. Therefore a phase shifter (a network of XOR gates) is often used to de-correlate the output patterns of the LFSR. The response of the CUT is usually compacted by a multiple input shift register (MISR) to a small signature, which is compared with a known fault-free signature to determine whether the CUT is faulty.

Pseudo-Random Pattern Generation

A string of 0's and 1's is called a pseudo-random binary sequence when the bits appear to be random in the local sense, but they are in some way repeatable. The linear feedback shift register (LFSR) pattern generator is most commonly used for pseudo-random pattern generation. In general, this requires more patterns than deterministic ATPG, but less than the exhaustive test. In contrast with other method, pseudo-random pattern BIST might require a long test time and necessitate evaluation of fault coverage by fault simulation. This pattern type, however, has the potential for lower hardware and performance overheads and less design effort than the prior methods. In pseudorandom test patterns, each bit has an approximately equal probability of being a 0 or a 1. The quantity of patterns applied is typically of the order of 103 to 107 and is related to the circuit's testability and the fault coverage required.

Linear feedback shift register reseeding is an example of a BIST technique that is based on controlling the LFSR state. LFSR reseeding might be static that is LFSR stops generating patterns while loading seeds, or dynamic, so as to is, test generation and seed loading can precede simultaneously. The length of the seed can be any equal to the size of the LFSR (full reseeding) or less than the LFSR (partial reseeding). In [5], a dynamic reseeding technique that allows partial reseeding is proposed to encode test vectors. A set of linear equations is solved to obtain the seeds, and test vectors are ordered to facilitate the solution of this set of linear equations.

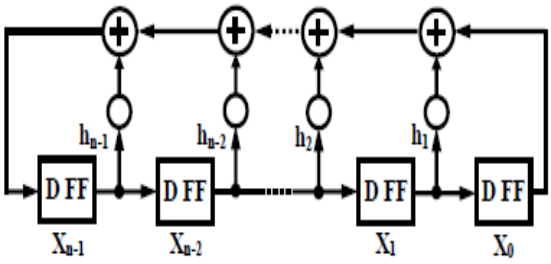


Figure 2 Standard LFSR circuit

COMBINATIONAL BENCHMARK CIRCUIT C432

Several Industry standard benchmark circuits such as ISCAS-85, ISCAS-89, etc can be used to test latest design, test and manufacturing approaches and technologies. Following is a brief explanation of one of the ISCAS-85 circuits used for the purpose of testing the new low power pattern generation system described above.

C432 is a 27-channel interrupt controller. The input channels are grouped into three 9-bit buses (we call them A, B and C), wherever the bit position within each bus determines the interrupt request priority. A forth 9-bit input (called E) enables and disables interrupt requests inside the respective bit positions. Figure below shows the c432 circuit. Figures show below the logic of the underlying modules.

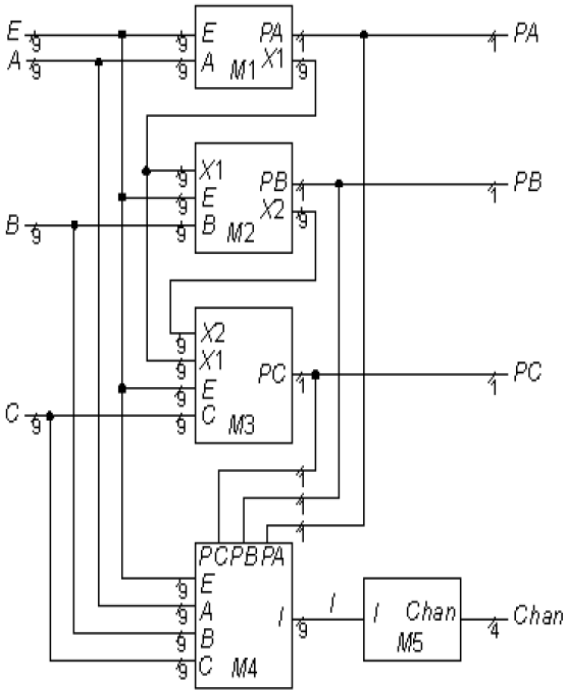


Figure 3 C432 Combinational Circuits

• Logic Gates are in use at Primary input combination in (2^36).

Statistics: 36 inputs, 7 outputs, 160 gates, bus translations

Function: c432 is a 27-channel interrupt controller. The enter channels are group into three 9-bit buses (we name them A, B and C), where the bit arrangement within each bus determines the interrupt request priority. A forth 9-bit input (called E) enables and disables interrupt requests within the particular bit positions. The figure above concisely represents the circuit. The figure above shown contains the modules labeled M1, M2, M3, M4, and M5, which contain the underlying logic.

Comparison of Test Generation Strategies

Implementing a BIST strategy, the main issues are fault coverage, hardware overhead, test time overhead, and design effort. These four issues have very complicated relationship. Table 1 summarizes the characteristics of the test strategies mentioned earlier based on the four issues.

Table 1 Comparison of different test strategies

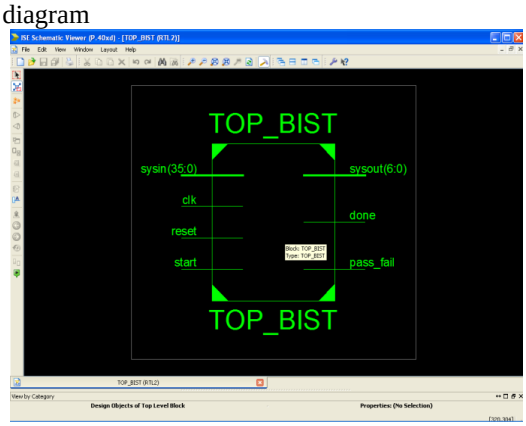
Test Generation Methodology	*Fault Coverage*	*Hardware Overhead*	*Test Time Overhead*	*Design Effort*
Stored Pattern	High	High	Short	Large
Exhaustive	High	Low	Long	Small
Pseudo-exhaustive	High	High	Medium	Large
Pseudo-random	Low	Low	Long	Small
Weighted Pseudo-random	Medium	Medium	Long	Medium

BIST Response Compression/Compaction Techniques

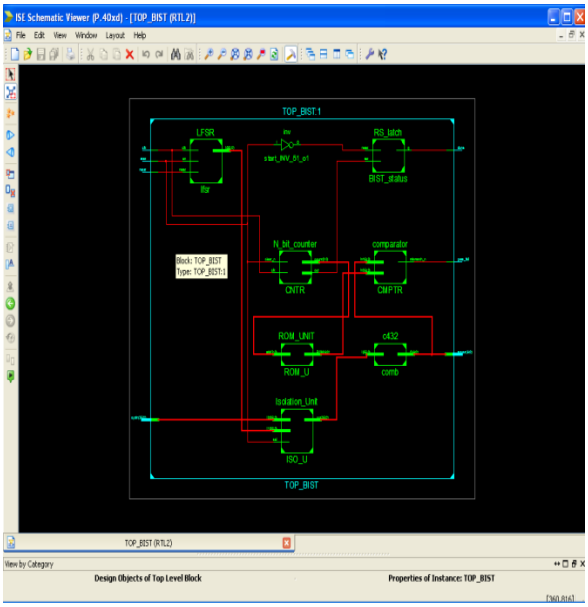
During BIST, large amount of data in CUT responses are applied to Response Monitor (RM). For example, if we consider a circuit of 200 outputs and if we want to generate 5 million random patterns, then the CUT response to RM will be 1 billion bits. This is not manageable in practice. So it is necessary to compact this enormous amount of circuit responses to a manageable size that can be stored on the chip. The response analyzer compresses a very long test response into a single word. Such a word is called a signature. The signature is then compared with the pre-stored golden signature obtained from the fault-free responses using the same compression mechanism. If the signature matches the golden copy, the CUT is regard fault-free. Otherwise, it is faulty. There are different response analysis methods such as ones count, transition count, syndrome count, and signature analysis.

III. RESULT ANALYIS

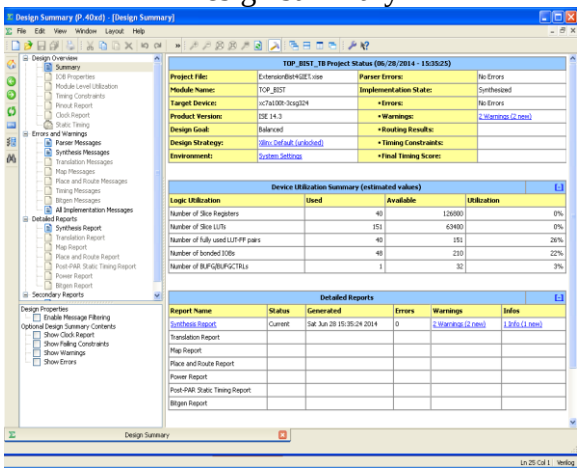
Block diagram



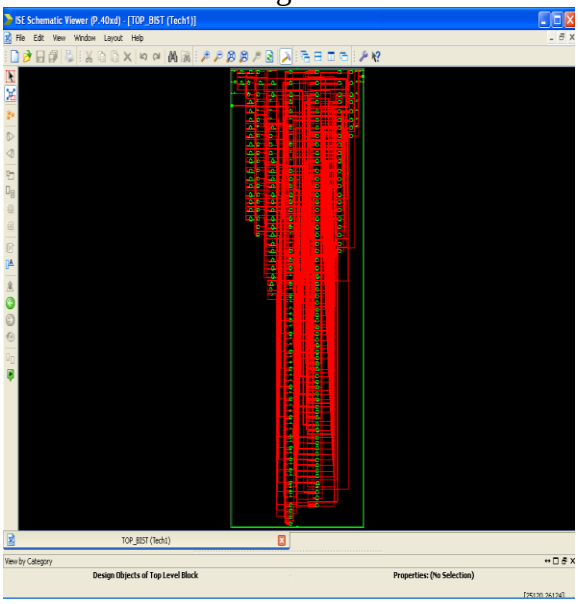
RTL schematic



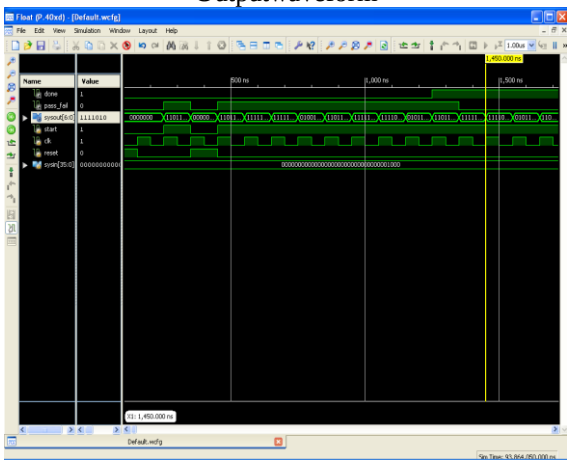
Design summary



Technology schematic diagram



Outputwaveform



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IV. CONCLUSION

The propose method implemented to test one of the combinational circuit by using Built in self test circuit. The presence of delay-inducing defects is causing increasing concern in the semiconductor industry today. To test used for such delay-inducing defects, scan-based transition fault testing techniques are being implemented. To Full scanning Process will Generated and then Fault coverage for Broadside testing is 80%, functional broadside testing is 40% and pseudorandom testing is 80%. Maximum length of testing full scan circuit is 402. Scanning percentage is 97%. Testing time for partial scan process is reduces Maximum testing length is reduced at 284.Here we were test the ISCAS-85 C432 27benchmark interrupt controller by using BIST circuit.

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AUTHOR'S DETAILS:

CHINTALAPUDI SRIKANTH TATAJI received her B.Tech Degree in ECE from Akula Sree Ramulu College of Engineering ,Tanuku West Godavari (Dt), in 2012. Presently, he is pursuing the M.Tech degree in Embedded Systems from JOGAIAH INSTITUTE OF TECHNOLOGY AND SCIENCES COLLEGE OF ENGINEERING Kalagampudi. West Godavari (Dt). At present, he is engaged in "DESIGN AND IMPLEMANTATION OF BIST FOR ISCAS-85 C432 COMBINATIONAL CIRCUIT ".

CH.KANAKALINGESWARARAO received the M.Tech degree from JNTUK, Swek, Jawaharlal Nehru Technological University, Kakinada in 2012. Currently he is working as Associate Professor in JITS Engineering College, Kalagampudi. He has ten years of experience in teaching.Previously he has worked in swarnadhra college of engineering, Narasapuram. His research interests FPGA Implementation of Scalable Encryption Algorithm