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DESIGN AND ANALYSIS OF EFFICIENT RECONFIGURABLE FIR FILTER USING CONSTANT MULTIPLIER ARCHITECTURE

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***Abstract*— Software Defined Radio and multi-standard video codec need a reconfigurable FIR filter with dynamically programmable filter coefficients. FIR Filter uses 2-bit BCSE technique and it requires more area and power. A reconfigurable FIR filter is designed by using a constant multiplier architecture based on VHBCSE algorithm. This design is used in multi-standard digital up converter (DUC) to reduce the power, delay and area consumption. The multiplexer and addition Unit in the final addition block of the constant multiplier architecture is replaced by programmable domain architecture. The number of multiplications and additions per input sample is initially reduced by using a programmable domain which is present in the DUC Filter architecture. This technique is capable of reducing the switching activity of the multiplier block adders. The Filter design and their parameters such as area, delay and power are analyzed using Xilinx tool. In this design the area is reduced to 30% and delay is reduced to 20% when compared to 2-bit BCSE technique.**

***IndexTerms*—coefficient, Digital up converter (DUC), finite impulse response, field programmable gate array,**

I. INTRODUCTION

FIR Filters are the signal conditioners. Each function accepts an input signal, blocking pre-specified frequency components and passing the original signal to the output. For example, the typical phone line will act as a filter that limits the frequencies range smaller than the range of frequencies human being can hear. Listening to the CD-quality music over the phone is not pleasing to the ear as doing it directly. A digital filter takes a digital input which will give a digital output and it consists of digital components. A Significant application of an efficient reconfigurable FIR filter will motivate the system designer to develop the chip with low power, low cost and the area along with the capability to operate at a very high speed.

The algorithms proposed earlier to implement an efficient FIR filter design can be categorized in two main groups: 1) Graph based algorithms 2) Common sub-expression elimination (CSE) algorithms [1]. In this paper the VHBCSE and 2-bit BCSE algorithm has been applied.

II. RECONFIGURABLE FIR ARCHITECTURE

The block diagram for the reconfigurable multiplier Architecture is shown in Fig.1. In this architecture, there are two parameters INTP_SEL and FLT_SEL which are used to select different interpolation and roll-off factors operations respectively.

The master clock (CLK) which is used to give the sample output (RRCOUT), this will operate at a higher rate than other three clock sources CLK divided by CLK4, CLK6, and CLK8 respectively. This will be used for sampling the serial input data for the different interpolation factors. Here, the proposed reconfigurable RRC filter architecture consists of major modules such as a coefficient generator, a data generator, a coefficient selector and an accumulator unit block.

A. Data Generator Block

DG block in Fig.1 is used to sample the input data depend on the selected value of the interpolation factor and the selection parameter. From the design of RRC filter, it has been observed that the values 25, 37, and 49[2] tap filters with the interpolation factors of four CLK, six CLK, and eight CLK constitute a branching filter of seven taps. This will indicate that the seven sub-filters are required for the multiplication of the filter coefficients with all the input sequence.

B. Co-efficient Generator Block

The CG block of the architecture performs the multiplication operation between the inputs and the filter coefficients. In this, the two-phase optimization technique is proposed which will help in reducing the hardware use by a significant amount to facilitate the reconfigurable FIR filter implementation with the low computation time and complexity.

The constant multiplier architecture is given in [5]. The planned multiplier considers the corresponding length of the input and coefficient will be 16-bit will be stored directly in the LUTs. In this, along with the hardware architecture, the different blocks of the designed VHBCSE based on the multiplier explained below. The multiplier architecture consists of major modules such as PPG, sign conversion, multiplexer unit, Controlled addition at layer 2&3, Final Layer. The data flow diagram of the constant multiplier as shown in the Fig [3].

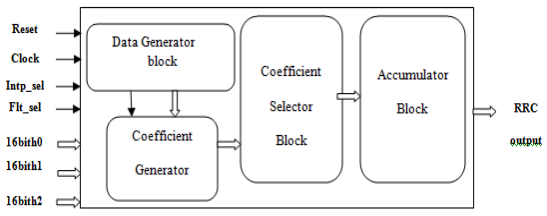


Fig.1 Reconfigurable FIR Filters

and 17-bit, while the output is assumed to the 16-bit long. The input value will be sampled and stored in the register first and then the coefficients will be stored directly in the LUTs. In this, along with the hardware architecture, the different blocks of the designed VHBCSE based on the multiplier explained below. The multiplier architecture consists of major modules such as PPG, sign conversion, multiplexer unit, Controlled addition at layer 2&3, Final Layer. The data flow diagram of the constant multiplier as shown in the Fig [3].

C. Sign Conversion Block

Sign Conversion Block (SCB) is needed to support the signed decimal format data which will be the representation of both the input and the coefficient values. The designed architecture of the sign conversion block is shown in [5].There is one complement circuit in-order to generate the inverted version of the 16-bit (excluding MSB) coefficient. One 16-bit of 2:1 multiplexer produces the multiplexed coefficients depending upon the value of the Most Significant Bit (MSB) of the coefficient. For negative value output of the original coefficient will be in the inverted form otherwise it will be as it is before.

D. First Coding Pass

In one FCP block, there are two sets of 25-, 37-, and 49-tap filter coefficient values which will differ only by the roll-of-factor are the input values. Inside the FCP block, there are three coding pass (CP) blocks which are running in parallel for the three different interpolation factors. The incidences of matching between all bits are explored vertically between the two coefficients of the same length filter. The architecture for implementation of FCP block is given in [2].

E. Second Coding Pass

The outputs from the First coding pass (FCP) blocks are the three sets of coded coefficients will passed through another CP block in-order to get the final coefficient set. In second coding pass (SCP), the common terms are present vertically in between those three coded coefficient sets will be find out and coded consequently. The architecture for implementation of SCP block is given in [2].

F. Partial Product Generator (PPG)

In this BSCE method, the shift and add based technique will be used to generate the partial product which will be calculated by using the following steps for producing the final multiplication result. The choice of the size of the BCS will define the number of the partial products. In the proposed algorithm, the layer-1 and the 2-bit binary common sub-expressions (BCSs) are ranging from"00" to "11" will be considered, which will produce four partial products. But, within the four of these BCSs, a single adder will be required to generate the partial product only for the pattern "11", and then rest of the product will be generated by hardwired shifting. And for the coefficient of the 16-bit length, eight partial product 17, 15, 13, 11, 9, 7, 5, and 3 bits (P8-P1) will be generated by the right shifting of the first partial product(P8) by the bits 0, 2, 4, 6, 8, 10, 12 and 14 respectively. The architecture of partial product generator block is given in [5].

G. Control Logic Generator

The Control Logic Generator block will take the multiplexed coefficient from the input and produce the 7 control signals which will depend on the equality checker for 7 different cases. The architecture of the Control Logic Generator block is shown in [5]. The control indicator for the 8-bit equality checker will be seen to produce through the control signals generated from the 4-bit equality check. The addition layers 2 and 3 are controlled by this control logic generator.

H. Multiplexers Unit

The Multiplexer unit will be used to select the proper data generated from the partial product generator unit which will depend upon the coefficients of the binary value. At layer-1, eight 4:1 multiplexers are required to produce the partial products according to the 2-bit BCSE algorithm. The width of these 8 multiplexers are 17, 15, 13, 11, 9, 7, 5 and 3-bit each instead of 16 –bit for all partial products, which will reduce the power and hardware consumption.

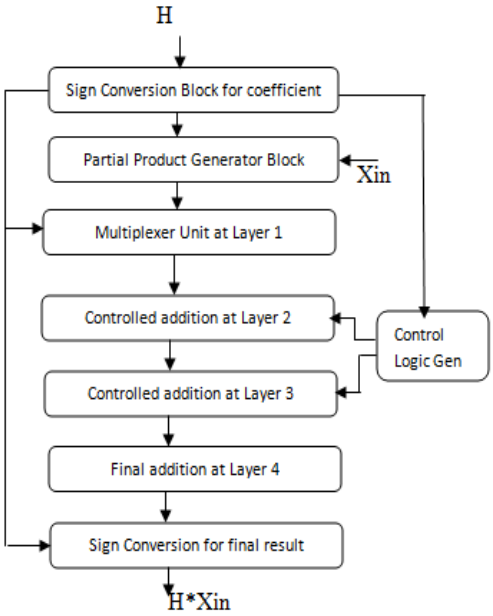


Fig.2 Data Flow diagram of the Co-efficient Multiplier

I. Controlled addition at layer-2

The Partial Products (PP) which generates from the eight groups of 2-bit BCS's are added to the final multiplication results which will perform in three layers. The architecture of controlled addition at layer-2 is given in [5].According to the BCSE algorithm the proposed layer 2 requires the four addition (A1-A4) operations to add the eight Partial products; the controlled addition operation is performed at the layer 2 in the case of the proposed VHBCSE algorithm. This address (A1-A4) will be controlled by depending on the control signals (C1-C6), which will generate based on the 4-bit BCSE from the Control Logic Generator block.

J. Controlled Addition at layer-3

The four multiplexed sum results (AS1, AS2, AS3 and AS4) are generated from the layer-2 which is now added up in the layer-3. In our algorithm, controlled additions are

performed, instead of direct addition of these four results will show in the Fig.9.Hence, this addition (A6) is controlled by the Control Signal (C7) from the CG block. The architecture for controlled addition at layer-3 is given in [5].

K. Final Addition on Layer-4

This Final Addition block on Layer-4 performs the addition operation between the two outputs (AS5- AS6) produced by layer-3 in-order to produce the final multiplication result between the input and the coefficient.

L. Coefficient Selector

In the case of the reconfigurable FIR filter, the coefficient selector block is used to select the proper data to the final build-up unit block depends on the particular interpolation factor parameter. It will take the input from coefficient Generator block. The architecture of Coefficient selector block is given in [2].

M. Final Data Accumulation Unit

The proposed reconfigurable FIR filter will be based on the transposed direct form of the architecture. The last accumulation block has the chain of six registers and six adders with the seven sub filters.

III. HARDWARE IMPLEMENTATION RESULTS AND DISCUSSIONS

The VHBCSE algorithm is based on the constant multiplier architecture that has been coded using the Verilog hardware description language (VHDL) to synthesize the FPGA Virtex-5 device which is using the Xilinx ISE 10.1i synthesis tool. The results will be as shown below. The Xilinx Power EDA tool is used to calculate the power consumption of each filter based on the switching activity which will be run by the designs clock. The particular area calculated for the reconfigurable Fir filter is shown in the following Fig.3. The final power for FIR filter is shown in the following Fig.4.

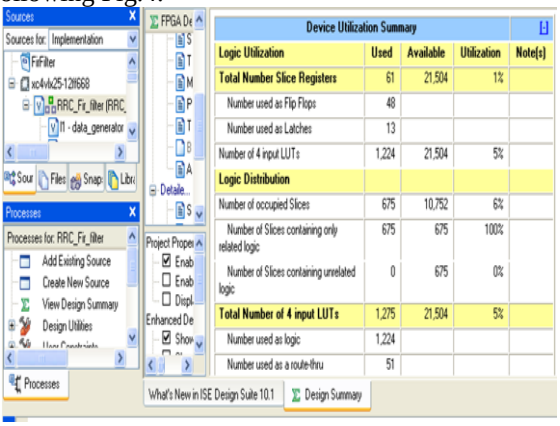


Fig. 3 Area for the Reconfigurable FIR Filter

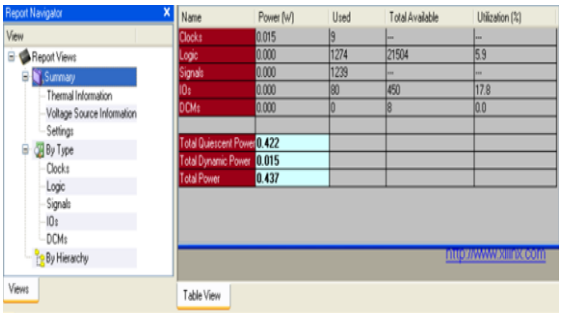


Fig. 4 Power for the Reconfigurable FIR Filter

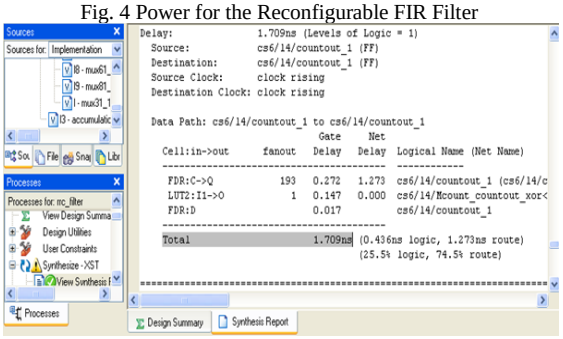
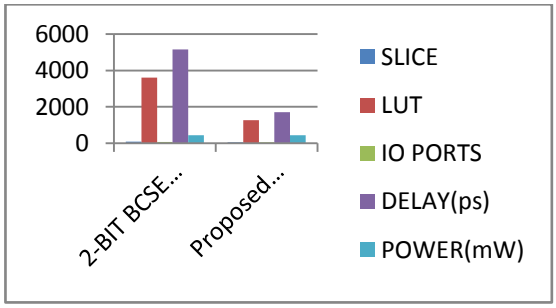


Fig.5 Delay for the Reconfigurable FIR Filter

IV. TABLE AND GRAPHS SHOWS IN COMPARISON RESULT BETWEEN TWO METHODS

Parameters	2-bit BCSE Architecture	Proposed architecture
SLICE	80	61
LUT	3610	1275
IO PORTS	77	60
DELAY	5.148ns	1.706ns
POWER	0.443W	0.437W



V. CONCLUSION

With a view to implementing an efficient fixed point reconfigurable FIR filter, this paper presents one new vertical –horizontal BSCE algorithm which removes the initial common sub-expressions by applying 2-bit BCSE perpendicularly. Further elimination of the CSs has been performed through finding the CSs present within the coefficients by applying BCSs of dissimilar lengths smoothly to unlike layers of the shift and add based constant multiplier architecture. It has been shown that the proposed algorithm successfully reduces the average switching activities of the multiplier block adder. Reduction of switching activities during hardware implementations of different FIR filters results in lowering the average power consumption. Implementation results reveal that there are considerable amount of power savings for higher order filter

as a large number of matches can be found for number of coefficients.

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