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A SURVEY ON DIFFERENT ARCHITECTURE FOR XOR GATE

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***Abstract*— Moore's law explains the necessity of the transistors for VLSI design. According to Moore's law "The number of transistors double once in every eighteen months". It gives the realistic observation that increase in number of transistors leads to increase in power dissipation of the system. This cause a major complication for the designers hence from there researchers are examining that how the circuit can be altered so that power consumption can be reduced. The design of code converters which forms the basic building blocks of all digital VLSI circuits has been undergoing a substantial improvement, being motivated by basic design goals, viz. minimizing the number of transistor, minimizing the power consumption. The XOR gates form the fundamental building block of code converters. In this paper Binary to Gray code converter is implemented by using 3,4,6 and 8T transistor of XOR gates and power dissipation is compared. Here designing is done under Micro wind software and XOR gates are designed using 3, 4 ,6& 8T (transistor). Each schematic designing is done under DSCH3 (a sub part of Micro wind) tool with respect to that simulation are performed.**

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I. INTRODUCTION

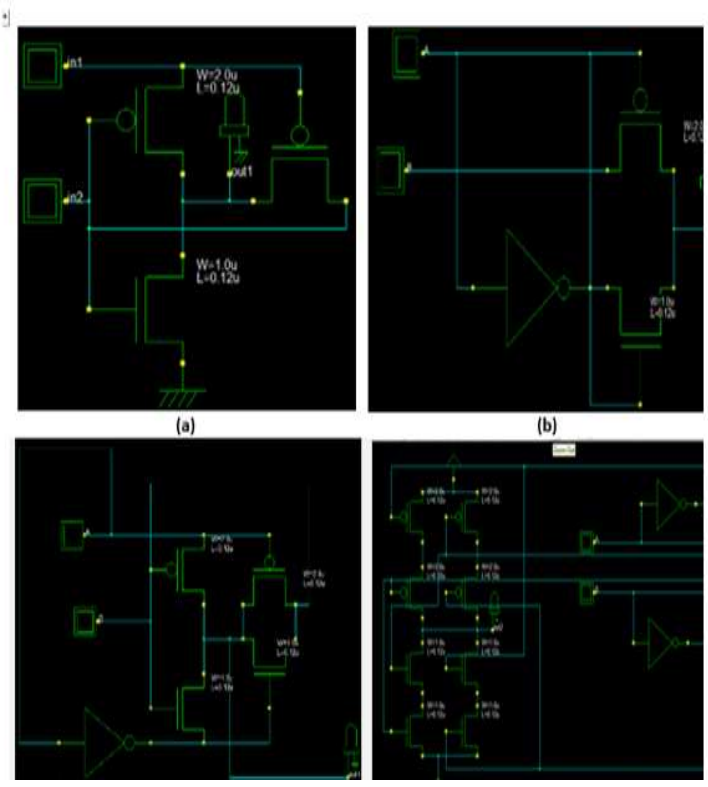
Various types of XOR gates that have been achieved over the years. The code converters are more power consuming circuits in digital design. To minimize the power dissipation several code converters are designed but they are not good enough for operation in the sub threshold region. These designs need large number of transistors, so these are not suitable for small and low-price systems. The power consumption techniques are CMOS complementary logic, Pseudo NMOS, Dynamic CMOS, Clocked CMOS logic (C2MOS), CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL).

The most useful low power consumption technique is PT. The PTL advantages are,

- Greater speed, due to small node capacitances.
- Low power dissipation, as a result of reduced number of transistors.
- Input can be applied to source/drain terminals as well as gate. This reduces the number of transistors required to implement a logic.

II. IMPLEMENTATION OF XOR GATE:

The basic building gate of binary to gray code converter is XOR gate. This gate forms the basic building blocks of many digital VLSI circuits. Improving the performance of the XOR gates can significantly enhances the performance of the system. The design of XOR gate has been undergoing a major improvement in power consumption. Many design techniques and frameworks have been established to reduce power consumption and has become one of the primary targets of digital design. In this paper we implement a Binary to Gray code converter by using 3,4,6 and 8T transistor of XOR gates.

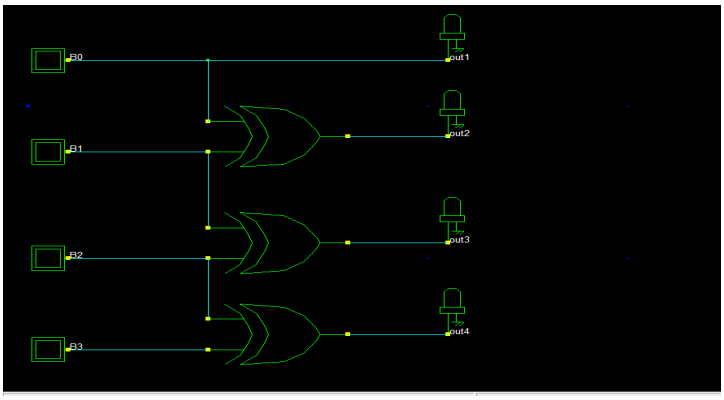


XOR gate with (a) 3T (b) 4T (c) 6T (d) 8T

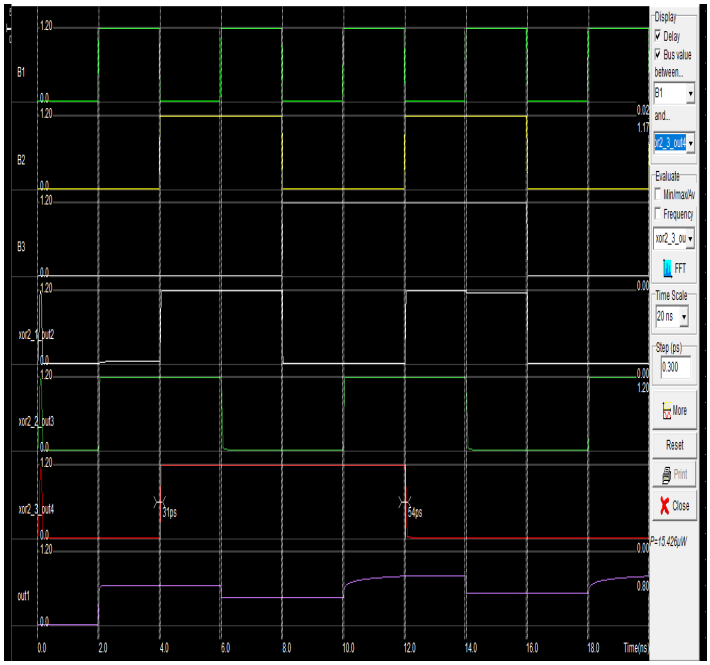
III.BINARY TO GRAY CODE CONVERTER

A binary code is a way of expressing text or computer processor commands using the binary number system as two binary digits 0 and 1. This is achieved by assigning a bit string to each symbol or instruction. Example, a binary string of eight binary digits can act as any of 256 possible values and so correspond to a collection of different symbols, letters or instructions. In telecommunication and computing, binary codes are used for any of a different methods of encoding data, such as character strings, bit strings. such methods may be fixed-width or variable width. In a fixed-width binary code, each digit, letter or other character, is expressed by a bit string of equal length; that bit string, interpreted as a binary number, is usually displayed in code tables in octal, decimal notation or hexadecimal notation. The reflected binary code, also known as Gray code. It is a binary numeral system where two successive values differ in only one bit. It is a non-weighted code. The reflected binary code was originally designed to prevent false output from electromechanical switches. Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems. Patent applications give "Gray code" as an alternative name for the "reflected binary code". one of those also lists "minimum error code" and "cyclic permutation code" among the names. The problem with natural binary codes is that, with real (mechanical) switches, it is very unlikely that switches will change states exactly in synchrony. In the transition between the two states, all three switches change state. In the brief period while all are changing, the switches will read some false position. Even without key bounce, the transition might look like 011 — 001 — 101 — 100. When the switches appear to be in position 001, the observer cannot tell if that is the "real" position 001, or a transitional state between two other positions. If the output feeds into a sequential system (possibly via combinational logic) then the sequential system may store a false value. The reflected binary code solves this problem by changing only one switch at a time, so there is never any of uncertainty position.

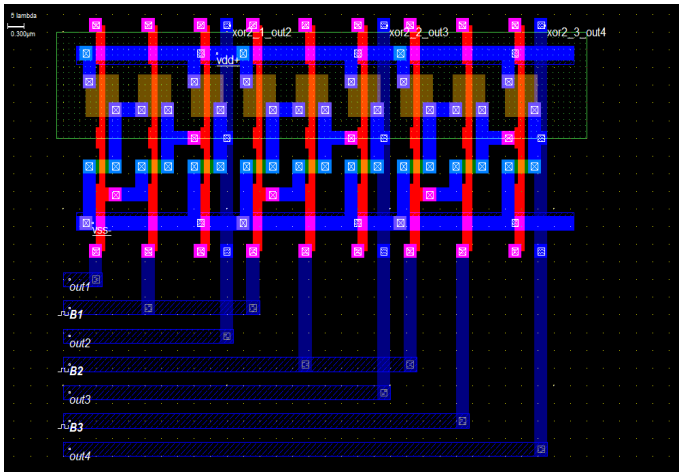
Decimal	Binary code	Gray code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100



(a)Binary to gray code using XOR gate



(b)simulated waveform of binary to gray code



(c) Layout diagram of Binary to Gray code

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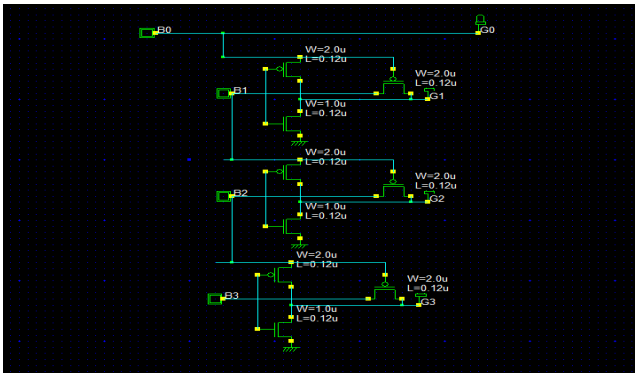
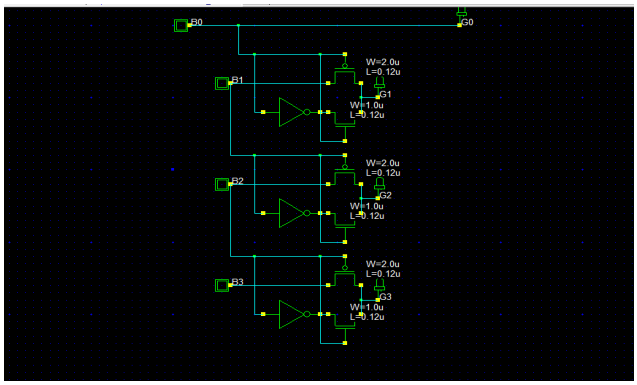
IV.DESIGN IMPLEMENTATION USING MENTOR GRAPHICS

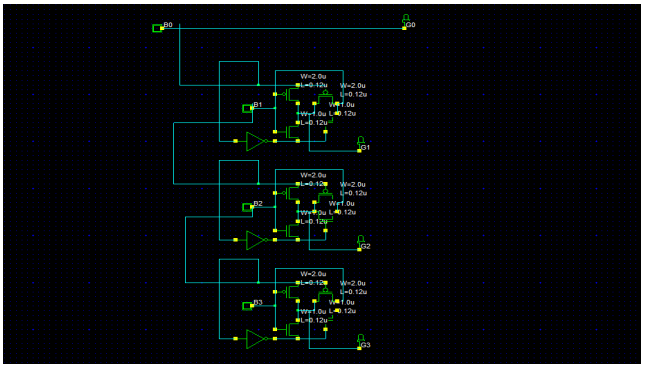
The basic building gate of binary to gray code converter is EX-OR .The designs of eight transistors ,six transistor,four transistor and three transistors binary to gray code using XOR gates are shown in figure. The digital VLSI circuits has undergone a considerable improvement, being motivated by basic design goals, viz.reducing the transistor count, reducing the power consumption.when we compare all the transistors 3T dissipates less power . The design of 3T transistor is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter functions as a CMOS inverter. When the input B is at logic low, the CMOS inverter output is at high impedance. Thus, the pass transistor is enabled, and the output Y gets the same logic value as input A. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across transistor and the output Y is degraded with respect to the input. Therefore, the design of 3T transistor gives the better performance.



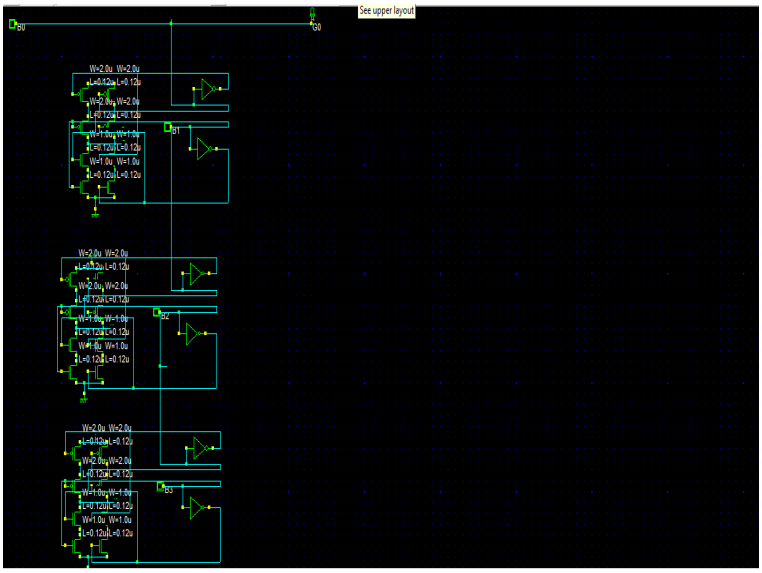
(a) Design of 3T XOR gate



(b) Design of 4T XOR gate

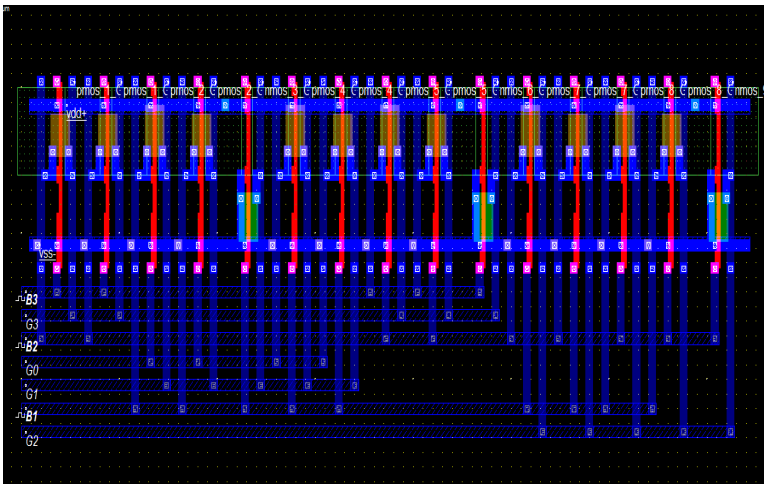


(c) Design of 6T XOR gate

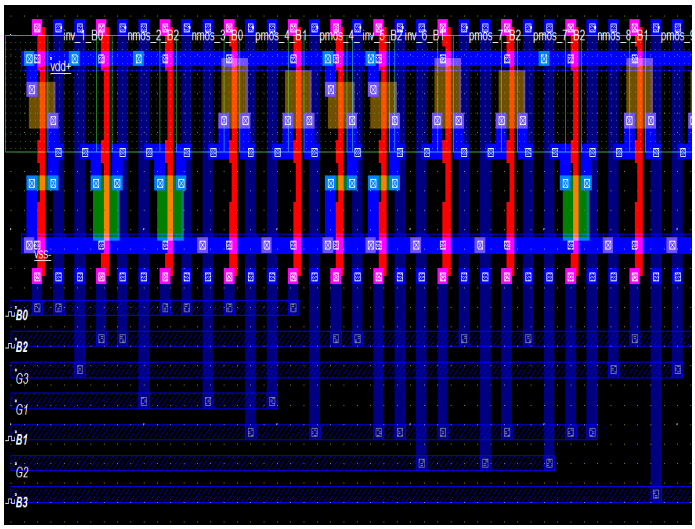


(d) Design of 8T XOR gate

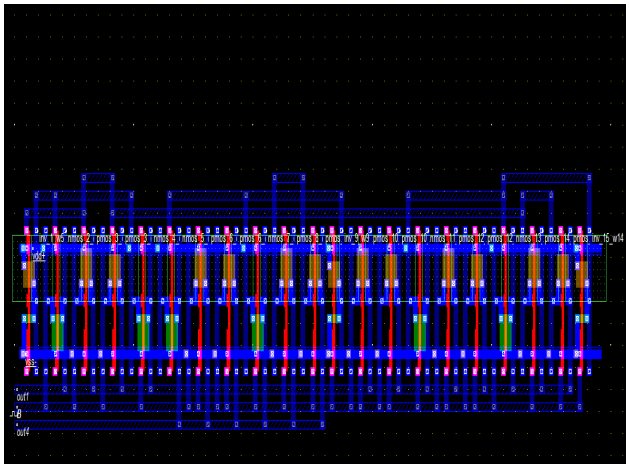
v. LAYOUT DIAGRAM OF BINARY TO GRAY CODE



(a) Layout diagram of 3T XOR gate

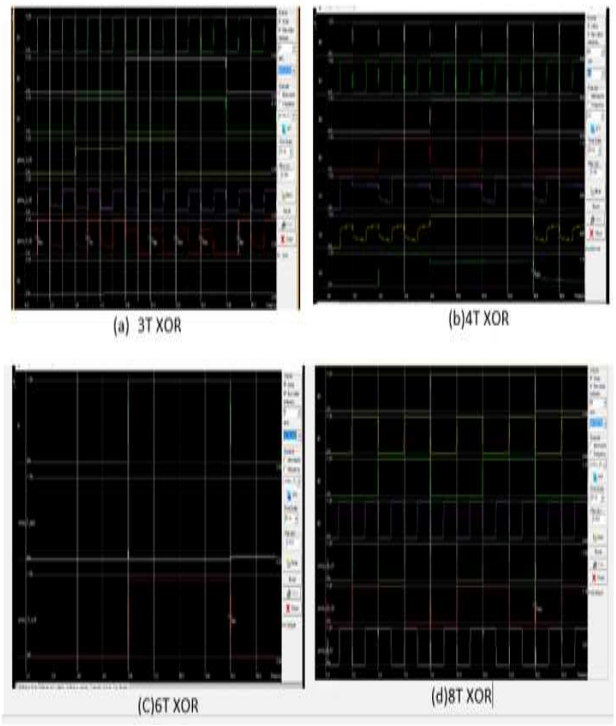


(b) Layout daigram of 4T XOR gate



(c) Layout diagram of 6T XOR gate
(d) Layout diagram of 8T XOR gate

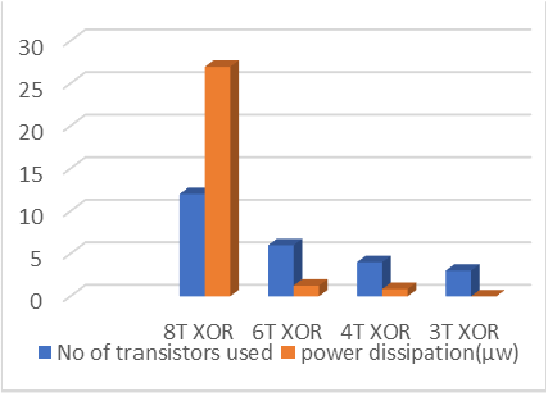
VI. SIMULATED WAVEFORMS OF XOR GATE



SIMULATED WAVEFORMS OF (a) 3T (b)4T (c) 6T (d) 8T XOR GATE

VII. RESULT AND DISCUSSION

The Binary to Gray code converter operates in 66 MHz range. In Mentor Graphics Tool both EX-OR and Binary to Gray code converter are designed. After that we were simulated these designs. By using simulation results we got the value of power dissipation and we were taken the input and output simulated waveforms. Thus, the simulated waveforms are shown in figure. The table shows the transistor count and power dissipation. From the table we can see that the decrease in number of transistor decreases the power dissipation. The Bar chart compares the number of transistors used and the power dissipation(µW).



Graphical presentation of simulation result

Table: Simulation result on layout of Binary to Gray code converter

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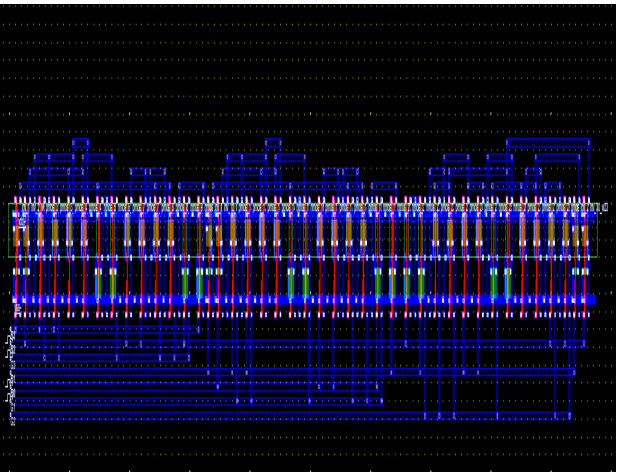
S:no	Design styles	No of transistors used	Power dissipation(µw)
1	8T XOR	12	26.952
2	6T XOR	6	1.263
3	4T XOR	4	0.851
4	3T XOR	3	very low (nW)

The number of transistors used for the XOR gate and the Binary to Gray code converter, obtained from the schematic representation is as shown in Table. From the simulated waveform the 3T XOR gate gives a better performance when compared to the other designs using8T, 6T and 4T XOR gate. Here XOR gate is used for design implementation which reduces the power dissipation due to less number transistors used. As the XOR gates form the fundamental building block of code converters, improving the performance of the XOR gates can significantly enhance the performance of the code converters.

VIII. CONCLUSION

A new technique, Binary to gray code using 3T,4T,6T and 8T transitors of XOR gate technique has been adopted for reducing the transistor count with full swing. These transistors have been implemented in Code Converters and the



comparison results have been shown. The performance metrics in terms of power dissipation and number of transistor are compared. The implementation of Binary to Gray Code Converter has been presented in XOR gates of 3T,4T,6T and 8T. The future research activities may include integration of the proposed Binary to Gray Code in complex digital systems, telecommunications and digital communication systems.

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