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PERFORMANCE COMPARISON OF CARRY SELECT ADDER WITH DIFFERENT TECHNIQUES

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***Abstract*— Design of high speed and low power data path logic systems is the most challenging areas of research in VLSI system design. Adder circuit is the main building block in DSP processor. However, Digital adders suffer with the problem of carry propagation delay. To alleviate this problem Carry Select Adder (CSLA) are used in computational unit. CSLA is a fast adder among other. CSLA is a high speed adder which is used to improve the speed of addition. The Square-Root Carry Select Adder (SQRT CSLA) design is simple but delay is high because of dual use of Ripple Carry Adder (RCA). The RCA has high delay than the full adder. To avoid such a high delay different techniques were used, a comparison is made on these techniques and some parameters were also compared with these techniques for different bit width.**

Keywords-component; delay, High speed, RCA, SQRT CSLA.

I. INTRODUCTION

Due to the rapid growth of portable electronic component the low power arithmetic circuits have become very important in VLSI industry. Multiplier-Accumulator (MAC) unit is the main building block in DSP processor. Full Adder (FA) is a part of the MAC unit can significantly affect the efficiency of whole system. Hence the reduction of power consumption of FA circuit is necessary for low power application. CSLA are used for high speed application by reducing propagation delay [1].

In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Among various adders, the CSLA is intermediate regarding speed and area. RCA provides the most compact design but takes longer computing time. If there is N-bit RCA, the delay is linearly proportional to N. Thus for large values of N the RCA gives highest delay of all adders [2].

RCA is constructed by cascading of Full adder which adds binary numbers. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}. A and B are the operands, and C_{in} is a bit carried in from the previous less significant stage. The circuit produces a two-bit output, output carry and sum typically represented by the signals C_{out} and sum [3].

In order to improve the shortcoming of RCA to remove the linear dependency between computation delay time and input word length, CSLA is presented. The dual RCA is used in CSLA structure. SQRT CSLA is recommended to avoid CPD in RCA. SQRT CSLA structure consists of dual RCA each one have C_{in} =0 and C_{in} =1.Dual use of RCA leads to high carry propagation delay (CPD). The CSLA is used in many computational systems design to moderate the problem of CPD by independently generating multiple carries and then select a carry to generate the sum [3].

CSLA uses independent RCA (for C_{in}=0 and C_{in}=1) to generate the resultant sum. However, the Regular CSLA is not area and speed efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry input. The final sum and carry is selected by the multiplexers (MUX). Due to the use of two independent RCA the area will increase which leads an increase in delay [4].

II. LITERATURE REVIEW

A. Square-root carry select adder using dual ripple carry adder

The basic idea of the CSLA is to use blocks of two RCA, one of which is fed with a constant "0" carry-in while the other is fed with a constant "1" carry-in. Therefore, both blocks can calculate in parallel. When the actual carry-in signal for the block arrives, MUX is used to select the correct one of both pre -calculated partial sums. Also, the resulting carry-out is selected and propagated to the next carry-select block. A CSLA is divided into sectors, each of which except for the least-significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder generally consists of two ripple carry adders and a MUX [4].

The CSLA is simple but rather fast, having a gate level depth. Adding two n-bit numbers with a CLSA is done with two RCA adders in order to perform the calculation twice, one time with the assumption of the carry being zero and the other

assuming one. After the two results is calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The RCA is constructed by cascading FA blocks in series. One FA is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage 4-Bit RCA. A serious drawback of this adder is that the delay increases linearly with the bit length [4].

Square-root (SQRT CSLA) is to implement large bit-width adders with less delay. In a SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The objective of SQRT CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay [5].

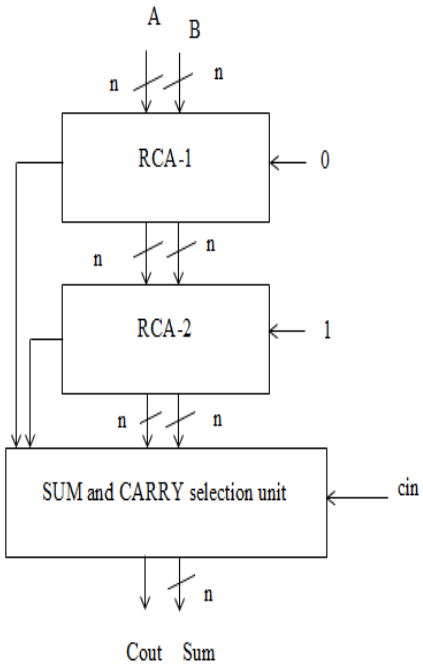

Figure 1. Square-Root Carry Select Adder

Each RCA block has two carry input one block has C_{in} =0, and other has C_{in} =1, the design is simple but carry propagation delay (CPD) is problem which make the design complex. Finally sum and carry is selected using multiplexer [5].

B. Square-root carry select adder using common Boolean logic

An area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional CSLA it saves many transistor counts and achieves a low power. Through analyzing the truth table of a single-bit full-adder, the output of summation signal as carry-in signal is logic "0" is the inverse signal of itself as carry-in signal is logic "1". For eg: S0 is "0110" as C_{in} is logic "0" and S0 is "1001" as C_{in} is logic "1". By sharing common Boolean logic term in summation generation, only need to implement one XOR gate with one INV gate to generate the summation signal pair. As the carry-in signal is ready and select the correct summation output according to the logic state of carry-in signal [6].

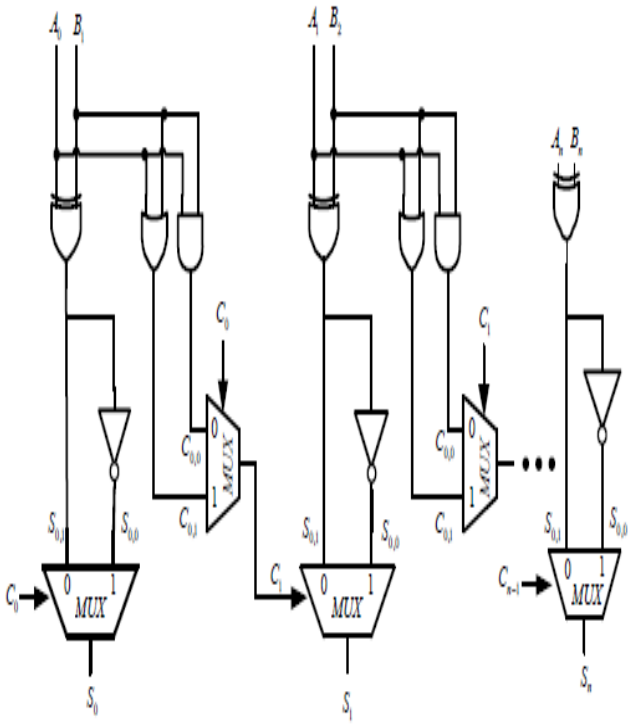

Figure 2. Square-Root Carry Select Adder with Common Boolean Logic

As for the carry propagation path, need one OR gate and one AND gate to anticipate possible carry input values in advance. Once the carry-in signal is ready, the correct carry-out output according to the logic state of carry-in signal. In this way, keep both the summation generation circuit of XOR gate and INV gate and the carry-out generation circuit of OR gate and AND gate in parallel [6].

C. Square-root carry select adder using BEC

CSLA is a fast adder which is used in digital communication and Memory Architectures. CSLA used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry is selected by the MUX. The basic idea of this work is to use Binary to Excess - 1 converter (BEC) instead of RCA with in the regular CSLA to achieve lower area and power consumption. The Carry of one RCA will be "0" and another will be "1". Here the output sum and carry is identified by the 2 to 1 MUX. The control signal of the MUX is carry C_{in} [8].

The CSLA are divided into two types: uniform sized adders and variable sized adders. If the bit length is equally divided it is called uniform sized adders. It is also called Linear CSLA. In variable sized adders the bit length are unequally divided. It is also called SQRT CSLA. Normally

the CSLA is designed with the Dual RCA with the carry being '1' and '0'. Here instead of having Dual RCA we are having only single RCA while the BEC is connected instead of RCA with Carry "1". The basic work of BEC in the regular CSLA to get lower area and improves the speed. This logic is replaced in RCA with C_{in}=1. This logic can be implements for different bits. The major advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit FA structure. The main idea of this work is to use BEC instead of the RCA with C_{in}=1 in order to decrease the area and increase the speed of operation in the regular CSLA to obtain modified CSLA. To replace the n-bit RCA, n+1 bit BEC logic is required [8].

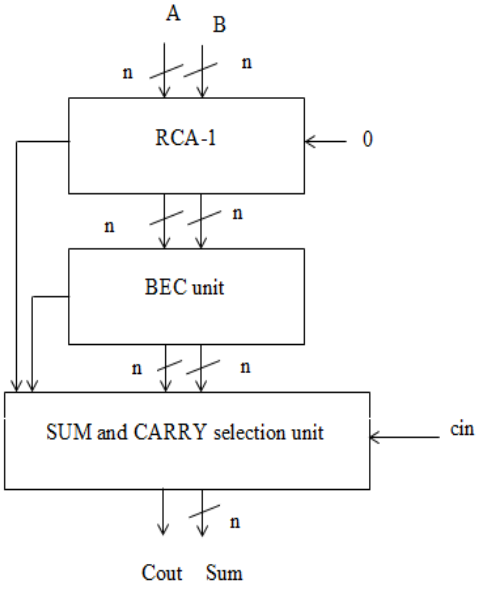

Figure 3. Square-root carry select adder with BEC

Table: Truth Table of BEC

INPUT A[0:3]	OUTPUT X[0:3]
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

D. Square-root carry select adder using add one circuit

SQRT CSLA use add one circuit instead of RCA with C_{in} =l, if the results of RCA with C_{in} = 0 is known, the result of RCA with C_{in} =l can be found by adding logic"1" to the result of C_{in} =0. An add one circuit can replace the RCA for C_{in} =l in a block. The 32-bit SQRT CSLA is designed using an add one circuit instead of a RCA with C_{in} =1 as shown in fig. 4.This architecture also consists of seven carry select stages (CSS). First CSS consists of only adders and remaining stages consist of adders, add one circuit, and first zero finding circuit and multiplexers [9].

The adders used in this architecture are mirror adders and eliminates inverters in the carry out path so delay in carry path is avoided. A MUX based add one circuit is used. A MUX is needed for each bit to choose in between sum and complement of sum. The main difference between a carry-select adder and a ripple-carry adder is that in a ripple-carry adder the carry has to ripple through all full-adders, but in the case of a carry-select adder the carry has to pass through a single MUX [9].

The control signal of the MUX is from the first zero finding circuit. The first zero finding circuit is NMOS and PMOS chains. This circuit generates "0" at the kth node if no zero is founded until kth bit from the least significant bit; otherwise, it generates "1". If the control signal is "0", the MUX chooses sum otherwise, it chooses the inverted sum. The least significant bit does not need a MUX since S^1_0 is always the opposite of S^0_0. This saves a few transistors for each block. An efficient design of an add one circuit, the area of SQRT CSLA with BEC can be further reduced when compared with SQRT CSLA. Complement scheme is used for designing add one circuit. Complement scheme states that, adding one is just inverting each Sum bit starting from the least significant bit until the first zero is found [9].

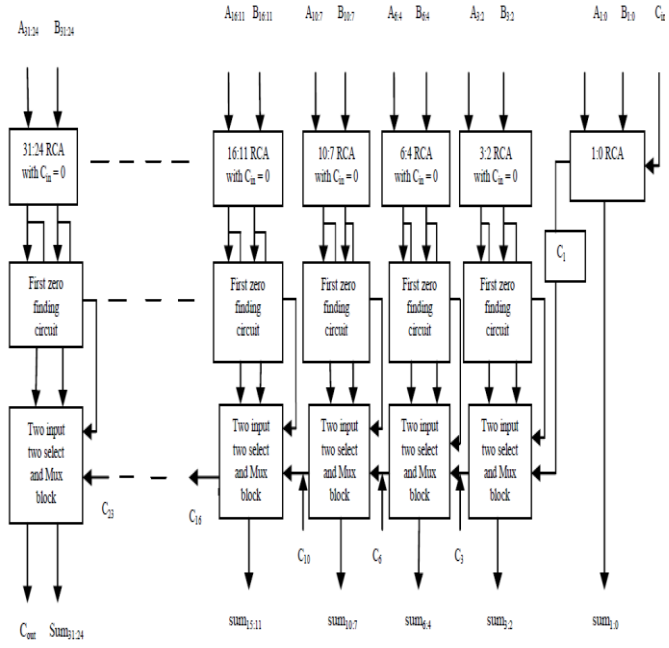

Figure 4. 32-bit SQRT CSLA with add one circuit

An efficient design of an add one circuit the area of SQRT CSLA with BEC can be further reduced when compared with SQRT CSLA. Complement scheme is used for designing add

one circuit. Complement scheme states that, adding one is just inverting each Sum bit starting from the least significant bit until the first zero is found [9].

Table: Comparisons of different techniques in SQRT CSLA

s.no	Types of adders	Width(n)	Area(um^2)	Power(W)	Delay(ns)
1.	SQRT CSLA with dual RCA	16 bit	2890	30.56723	5.61
		32 bit	6100	60.2537	6.56
		64 bit	12613	113.6452	8.37
2.	SQRT CSLA with BEC	16 bit	2325	25.79	5.96
		32 bit	4801	50.07	7.64
		64 bit	9809	91.17	10.18
3.	SQRT CSLA with CBL	16 bit	1722	12.86	10.45
		32 bit	2765	17.79	18.72
		64 bit	5530	30.14	35.10
4.	SQRT CSLA with add one circuit	16 bit	589	-	4.85
		32 bit	1245	-	6.81
		64 bit	-	-	-

III. CONCLUSION

In this paper three digital adder techniques are discussed such as BEC, common Boolean logic and add one circuit which are used to reduce carry propagation delay and also used in applications such as DSP processor, microprocessor etc. In BEC the delay gets reduced by simple gate level modification likewise common Boolean logic and add one circuit has also less delay, when compare to CSLA common Boolean logic and add one circuit has less number of logic gates. A comparison is made on these techniques based on the parameter such as area, power and delay which improves speed of the addition.

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