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FPGA BASED SEQUENCER FOR ANALOG INPUT CARD WITH ISOLATION (AIC-ISO)

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***Abstract*— Analog Input card is used in embedded systems of safety critical, safety related and non-nuclear safety systems of Nuclear Power Plants. Analog Input Card with Isolation (AIC-ISO) receives the analog signal that is to be isolated, processed, stored and transmitted to specified destination. AIC-ISO is based on Versa Module Europa 64x bus (VME 64x). The FPGA based controller which reduces the CPU load is designed and it will be ported in the Analog Input Card with isolation. The card contains multiplexers, isolation amplifiers, low pass filter, Data Acquisition System (DAS) and sequencer. The received signal passes into multiplexer and isolated by isolation amplifier. The noise will be attenuated in the low pass filter then passes to the DAS chip. The FPGA based controller is been designed to provide control signals for multiplexer, VME 64x, DAS chip. The Sequencer has 3 major functionalities. They are DAS interface logic, memory, VME bus interface logic. These are coded in VHDL and stimulated in Libero soc Tool.**

Keywords—FPGA, VHDL, VME 64x, Simulation, Analog input card

I. INTRODUCTION

The Instrumentation and control (I&C) systems is very important in Nuclear power plants (NPP) for monitoring and controlling various parameters of the plant. These I&C systems are used for protection of the plant and the personnel. The conventional instruments are used to measure and control the process parameters of non-nuclear power plant like temperature, pressure, level, flow etc. In NPP, in addition to these instruments, special equipments are used to monitor neutron flux, radiation levels etc.

The Embedded systems take active part in design and development of I&C systems. I&C systems of NPP are categorized into three major categories such as safety critical, safety related and non-nuclear safety systems.

II. CATEGORIZATION OF I&C SYSTEM

A. Safety Critical Systems(SCS)

Safety critical systems play a principal role in achievement of nuclear power plant safety by safe shutdown of the reactor followed by heat removal from the core and containment of radioactivity.

B. Safety Related Systems (SRS)

Safety related systems play a complementary role in achievement or maintenance of nuclear power plant safety. The efficient operation of safety related systems reduce the demand on safety critical systems thus enhancing the availability of plant operation.

C. Non-Nuclear Safety systems (NNS)

Non-nuclear safety systems play auxiliary or indirect role in the achievement or maintenance of nuclear power plant safety. They can be part of total response to an incident but not be directly involved in mitigating the physical consequences of the incident.

III. LITERATURE SURVEY

At present VME 32 bus based Analog Input cards is used in embedded systems which does not have geographical addressing and hotswappability. Hence VME64x bus based AIC is designed to have hotswappablility that reduces the down time of the system. It also has geographical addressing which avoids address jumper setting. The backplane of VME 64x has 3 ports whereas VME 32 bus has only 2 ports.

IV. SPECIFICATION OF AIC-ISO

The following are the specifications of are AIC -ISO
- No of Channels: 8
- Type: Single / Differential
- Input Range: -10V to +10V / -5V to +5V
- High Input impedance
- High Common mode rejection ratio
- Bus Interface: VME A16/ D32
- Per channel isolation and calibration
- Isolation Voltage: 2.5 kV (input to output)
- ADC is provided with a resolution of 18 bits.
- Power Supply Requirement: +5 V

V. ANALOG INPUT CARD DESIGN

The block diagram analog input card with isolation is shown in the Fig.1.

A. Multiplexer

The front end devices of AIC-ISO are multiplexer. It is used for calibration purpose. In this card 4:1 multiplexer is used, first input of the multiplexer is connected to field signal,

second input is connected to reference input. Third and fourth input signals are connected to ground.

B. Isolation amplifier

AIC with isolation uses three-port isolation amplifier. This isolation amplifier provides complete isolation function from field and the controlling environment. The three-port design structure allows each port (input, output, and power) to remain independent. The isolation amplifiers provide protection from fault conditions that may cause damage to other section of a measurement system.

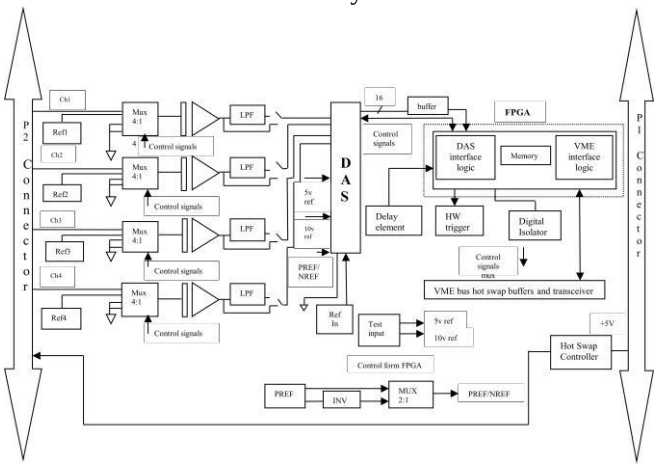

Fig. 1. Block diagram of Analog Input Card with Isolation

C. Low pass filter

Low pass filter is used for the removal of high frequency noise that is associated with the field signal.

D. Data acquisition system(DAS)

The DAS is the last link in the chain between the analog domain and digital signal path. It has high speed, low power, 18 bit successive approximation Analog to Digital Converter (ADC) and allows the simultaneous sampling of eight analog input channels. The sequencer logic generates control signals for DAS.

E. Sequencer

FPGA is used as a sequencing and control device in AIC -ISO. FPGAs are suited to process high speed and high channel density signals because they have multichannel synchronization and impressive digital processing performance.

VI. SEQUENCER IMPLEMENTATION

Sequencer is an FPGA based controlling device on AIC-ISO, designed to minimize the CPU load. VME bus interface logic, DAS interface logic and memory are integrated into single FPGA. Sequencer design is implemented on Actel device using VHDL language.

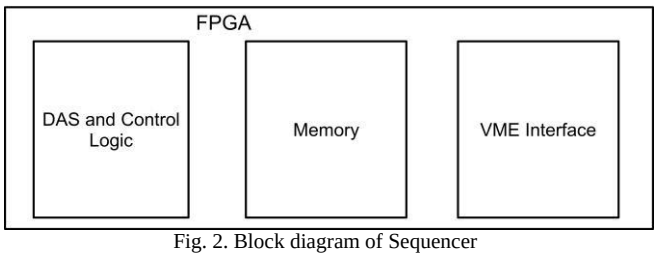

Fig. 2. Block diagram of Sequencer

It generates the control signals for devices such as multiplexers, DAS chip and VME interface. Sequencer is designed to scan 8 channels and store the scanned data in memory.The block diagram of sequencer is shown in Fig. 2.

The design flow of VLSI is shown in Fig.3

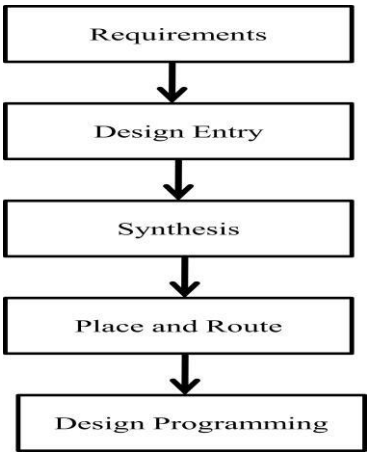

Fig. 3. Design flow of VLSI

A. DAS and Control logic

1) Features of DAS

- It has 8 simultaneously sampled inputs
- Analog input ranges: ±10 V, ±5 V
- Single 5 V analog supply and 2.3 V to 5.25 V VDRIVE
- It has 18 bit successive approximation type analog to digital converter
- Flexible parallel/serial interface
- Conversion time for 8 channels
  - ✓ 0.32 ms with oversampling
  - ✓ 5µs without oversampling

2) Block diagram and flow chart and of DAS interface

The block diagram of DAS interface and DAS is given in Fig. 4.

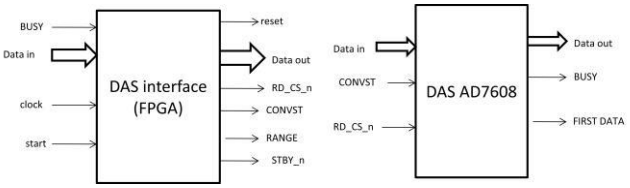

Fig. 4.Block diagram of DAS interface

Fig. 5 explains the flow chart of the DAS interface logic. The initialization of DAS chip is made and conversion start signal is issued from CPU. Once the conversion is over, it is indicated by the BUSY signal. The data is read by issuing the chip select and read signal (CS_RD_n), which is active low. Two read cycles are required to get 18 bits of each channel from DAS chip. In the first read cycle the data is read from 17:2 bits. And the remaining two bits (i.e.) 1:0 are read in the second read cycle. The number of channels is

incremented after reading each channel. Once 8 channels are read the loop is over and the process is terminated.

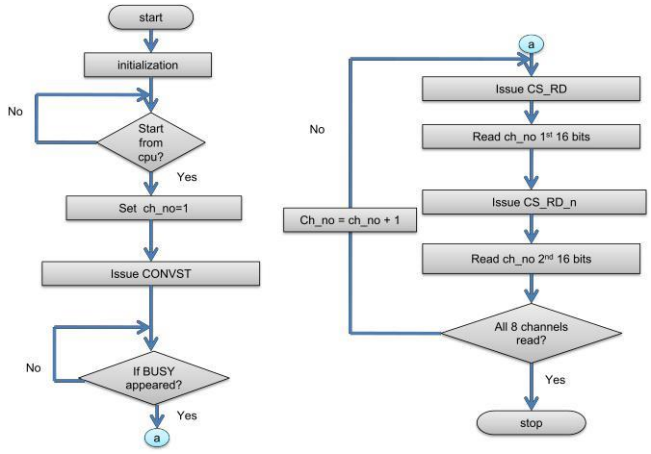

Fig. 5. Flow chart of DAS interface

B. Memory

- Memory is used to read and write data in a specified place which are used for further evaluations.
- The size of the memory designed is 16x16. (Number of locations x Number of bits per location)
- There are 8 channels with 18 bits in each channel. Since DAS requires two cycles to read 18 bit data. First 16 bit is stored in one memory location and second 16 bits are stored in the next location for each channel. The block diagram of memory is shown in Fig. 6.

1) Block diagram of memory

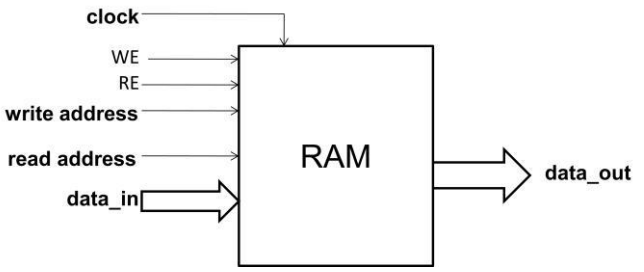

Fig. 6. Block diagram of memory

a) Write Process:

When the write enable pulse is high and the address is given, then the given input is written in the specified address.

b) Read Process:

When the read enable pulse is high and the address to be read is given, then the required data is given through data_out.

Table 1 gives the description of memory signals.

TABLE 1. Description of memory signals

Input / Output Signals	Description
RE	Read enable signal
WE	Write enable signal
Read address	Address lines to read in the memory
Write address	Address lines to write in the memory
Data_in (16 bits)	Data to be stored in the memory
Data_out (16 bits)	Data that is taken from the memory

C. VME interface

1) Features of VME bus

- VME - Versa module Europa
- VERSA-Module Euro card was introduced in 1981 for industrial, commercial and military applications.

- Master Slave architecture
- Non-multiplexed – Separate pins for Address and Data lines
- Asynchronous Bus - there is no clock used to coordinate the data transfer
- Flexible Address range and Data path width and can be selected dynamically
- Multiprocessing capability

2) Block diagram of VME interface

The main function of VME interface is to transfer the information between the CPU and the I/O cards. These are done by the read and write cycles.

The block diagram of VME interface containing geographical addressing & address modifiers decoding, board select generation and DTACK signal generation is shown is Fig. 7.

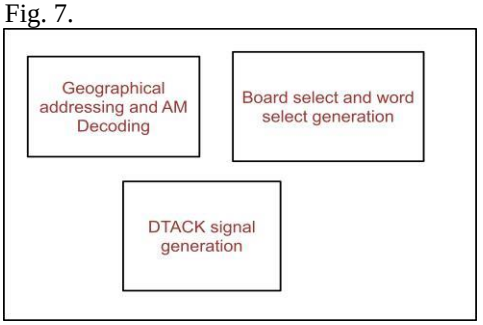

Fig. 7. Block diagram of VME interface

The other important signals used by the read/write cycle are given in Table 3.

TABLE 3. Signals of read/write cycle

Address	Data	Control
A01-A31 AM0-AM5 LWORD*	D00 – D31	AS* WRITE* DS0*,DS1* DTACK* BERR* RETRY*

VII. VHDL DESIGN

The combination of all the three blocks in a single program is known as hierarchical modeling. The pre synthesis simulation is done by the test bench written in VHDL.
The output of the sequencer is shown in Fig. 8.

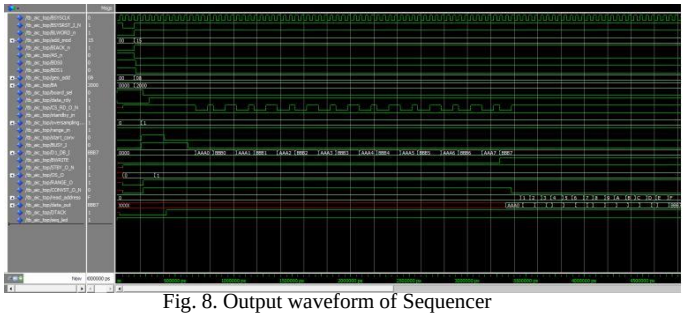

Fig. 8. Output waveform of Sequencer

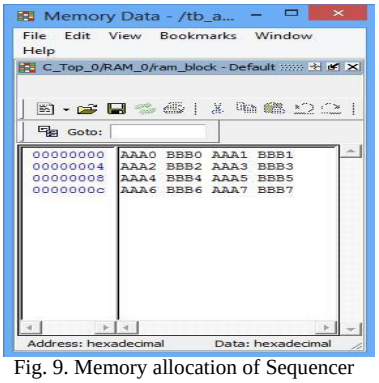

Fig. 9. Memory allocation of Sequencer

The simulated data are read by the DAS and stored in the memory. The allocation of memory for the simulated data is shown in Fig.9.
The sequencer design is synthesized. The block diagram of Synthesizer is shown in Fig.10

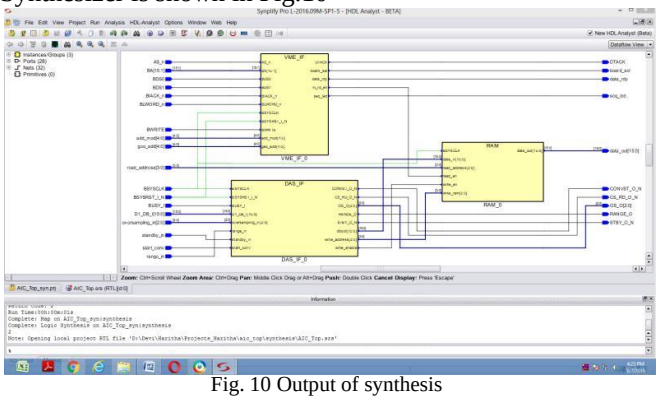

Fig. 10 Output of synthesis

VIII. FUTURE WORK

- Diagnostic of memory and DAS can be included in the sequencer,
- Interrupt cycle can be included of Analog Input Card with Isolation.
- Sequencer design has to be ported into AIC-ISO and tested.

IX. CONCLUSION

Sequencer for AIC-ISO is designed and developed in-house. Design is verified with test bench in ModelSim Tool.

X. ACKNOWLEDGEMENT

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