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A STUDY ON LOW POWER IMPLEMENTATION OF MULTIPLEXER

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***Abstract*— The aim of this work is to design a 2:1 multiplexer using Universal gates and CMOS logic. It compares the use of CMOS logic in the design of 2:1 multiplexer as more power efficient than NOR, NAND gates [5]. This demonstrates that the CMOS logic takes lead as it uses less transistors, have smaller capacitances and faster than others. In this paper a comparative study is made and the simulated result illustrates the superior nature of CMOS logic design as it dissipates very less power when compared to others. The designed circuits are implemented, stimulated and tested using the Microwind DSCH3 software tools.**

***Index Terms*—Moore's law, Universal gates, CMOS technology, Microwind, Layout**

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating integrated circuits (IC) by combining hundreds of thousands of transistors or devices into a single chip. VLSI technology is based on Moore's law. Moore's law refers to an observation that the number of transistors per square inch on integrated circuits has doubled approximately every 18 months [1]. This increase in number of transistors on ICs will reduce the power consumption.

Multiplexer is also called as data selector. A multiplexer is a combinational circuit that selects binary information from one to many input lines and directs it to a single output line. The 2:1 multiplexer circuit has one output, two inputs and one selection input. The selection of particular input line is controlled by a set of selection lines. The selection line determines which of the input bit is transmitted to the output. [2]

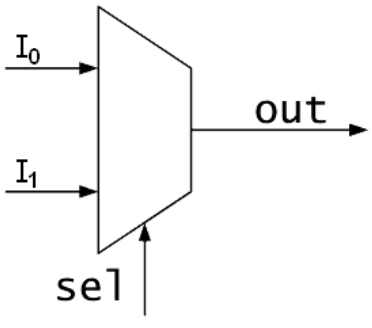


Fig. 1 2:1 multiplexer

Multiplexers can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analog types using transistors, or relays to switch one of the voltage or current inputs through to a single output. Examples for 2:1 multiplexer are IC 74157, IC 78158. In this paper design of 2:1 mux is made using NOR, NAND gates and CMOS logic and their corresponding power dissipation is compared. This paper is based on the power efficient design of 2 to 1 multiplexer using microwind tool.

II. DESIGN OF 2:1 MULTIPLEXER USING ONLY NOR LOGIC

The NOR gate is a digital logic gate. That produces a HIGH output if both the inputs to the gate are LOW; if one or both input is HIGH, a LOW output results [7]. NOR gates are basic logic gates such that they can be recognized in TTL and CMOS ICs. Here NOR gates are combined to generate the operation of 2:1 multiplexer. The schematic diagram of 2:1 mux using only NOR gates is shown in Fig. 2

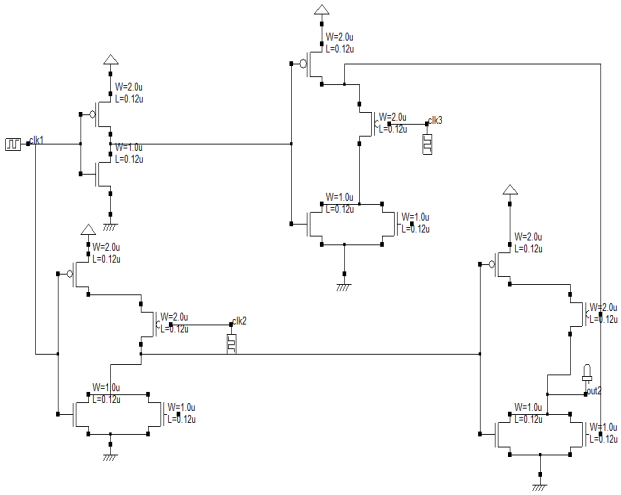


Fig. 2 Schematic of 2:1 mux using only NOR logic

This circuit is designed with the help of universal NOR gates. The total number of transistors used is 14 in which 7 are PMOS and 7 are NMOS. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when

both inputs are low [6]. The output is never left floating. The layout design is shown in Fig. 3. This design is more complex and consumes more area.

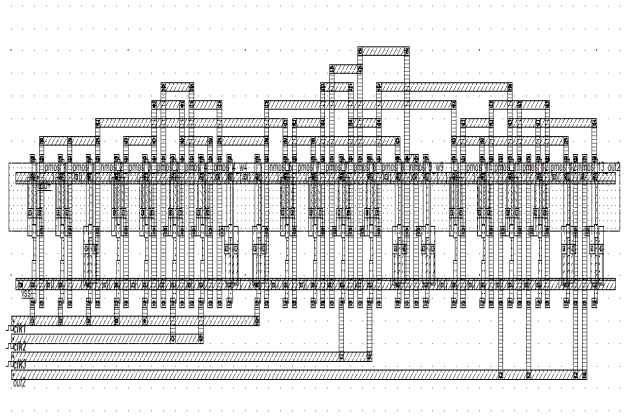


Fig. 3 Layout design

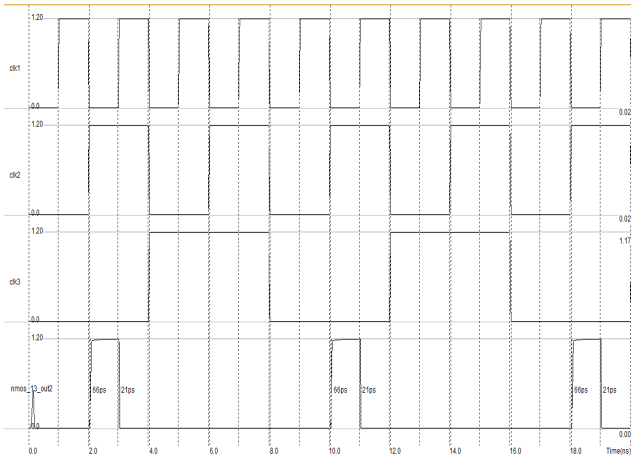


Fig. 4 Timing diagram

III. DESIGN OF 2:1 MULTIPLEXER USING NAND LOGIC

A NAND gate (negative-AND) is a logic gate which produces a LOW output only if both the inputs to the gate are HIGH; if one or both inputs are LOW, a HIGH output results[6]. Here 2:1 mux is designed using only NAND gates. The reason for moving to the use of NAND gates is that, it occupies less area when compared to NOR gates. The delay offered by NAND gates is less than that of NOR. NAND uses transistors of similar size where NOR do not. This will reduce the manufacturing cost of NAND gates as well as the power dissipation [3]. The schematic diagram of 2:1 mux using only NAND gates is shown in Fig. 5.

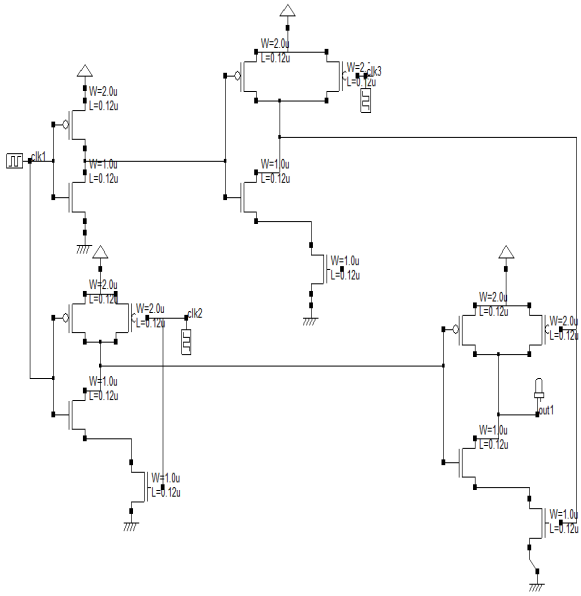


Fig. 5 Schematic of 2:1 mux using only NAND gates

The 2:1 mux designed using NAND gates has 7 NMOS and 7 PMOS totally 14 transistors. Here the NMOS transistors are connected in series and PMOS transistors are connected in parallel [5]. The layout design for the above circuit is shown in Fig. 6. This design is less complex and consumes less area than the NOR gates implementation. The power consumption is also reduced.

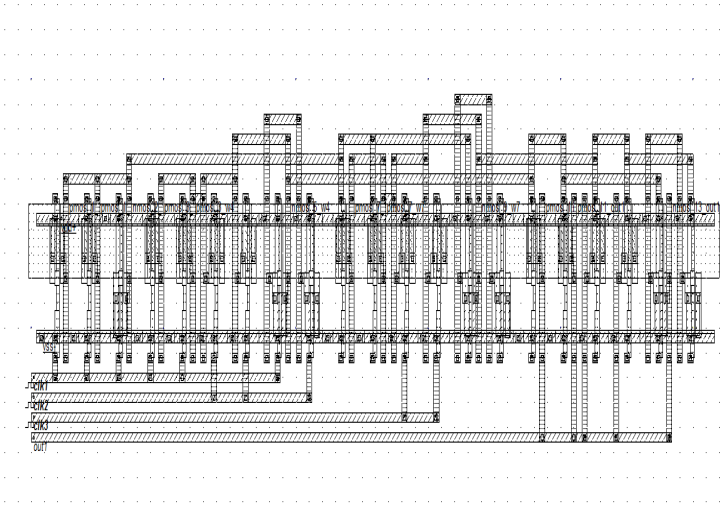


Fig. 6 Layout design

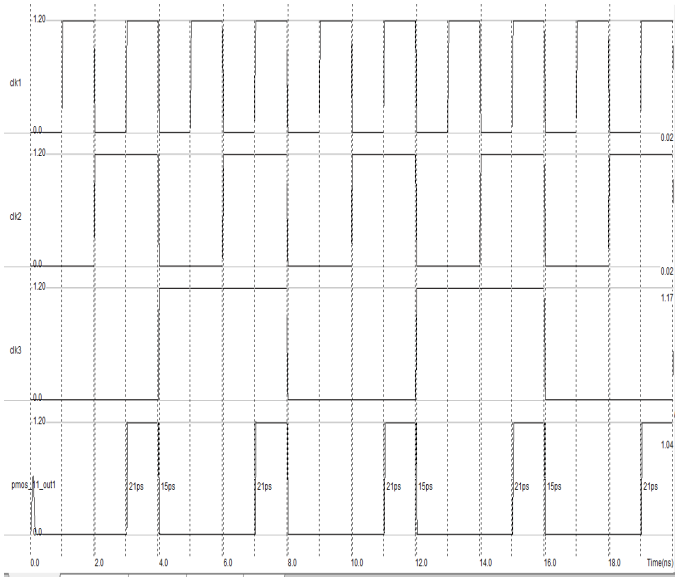


Fig. 7 Timing diagram

IV. DESIGN OF 2:1 MULTIPLEXER USING CMOS LOGIC

Complementary metal oxide semiconductor is the latest technology for constructing integrated circuits. This technology makes use of both P channel MOS (PMOS) and N channel MOS (NMOS) semiconductor devices. In NMOS, the majority carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct [3]. NMOS are considered to be faster than PMOS, since the carriers in NMOS, travel twice as fast as the holes. In PMOS, the majority carriers are holes. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices. The important characteristics of CMOS logic are high noise immunity and low power consumption. Since one transistor of the pair is always off, the series combination draws significantly less power and do not produce as much waste heat than other forms of logic[4]. The schematic diagram of 2:1 mux using CMOS logic is shown in Fig. 8

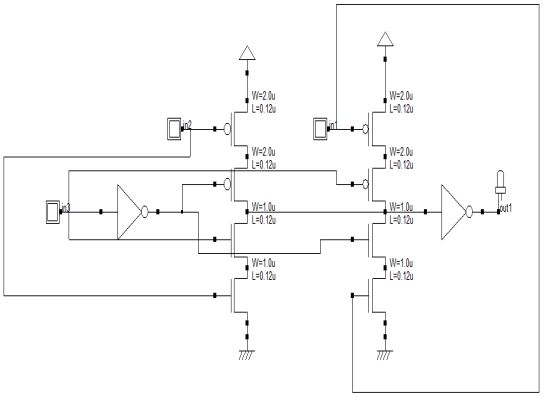


Fig. 8 Schematic of 2:1 mux using CMOS logic

In this design, the total number of transistors used is 8. The layout of 2:1 mux using CMOS logic is shown in Fig. 9. This design is very simple and consumes less area than the NAND logic. The power dissipation is very much reduced.

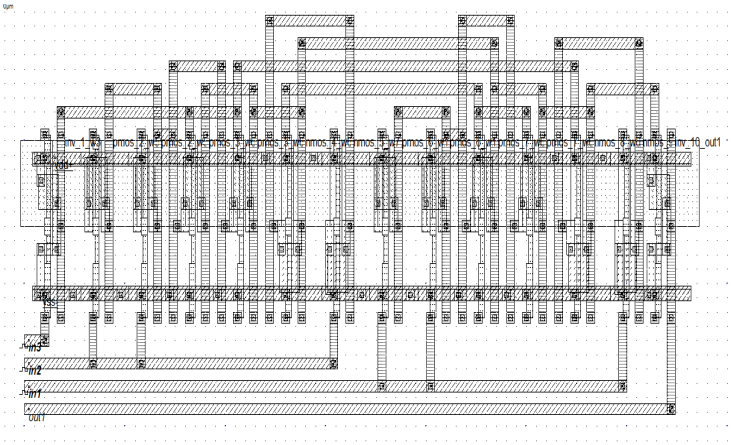


Fig. 9 Layout design

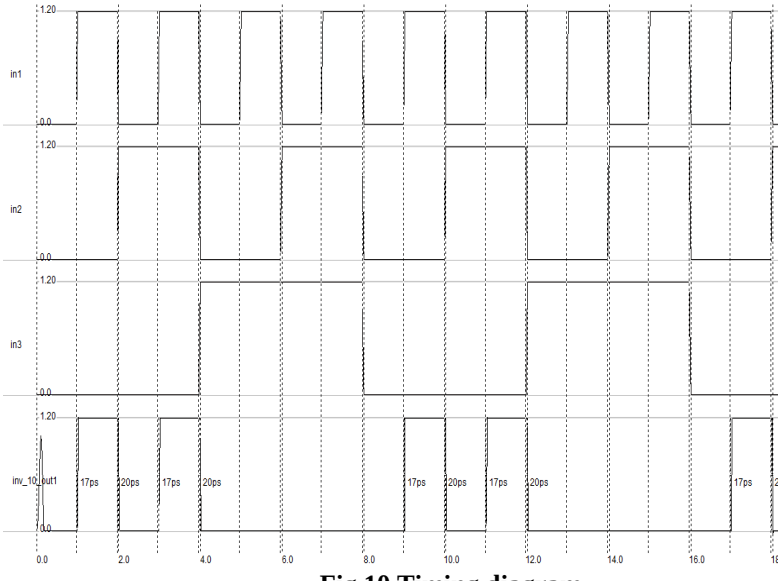
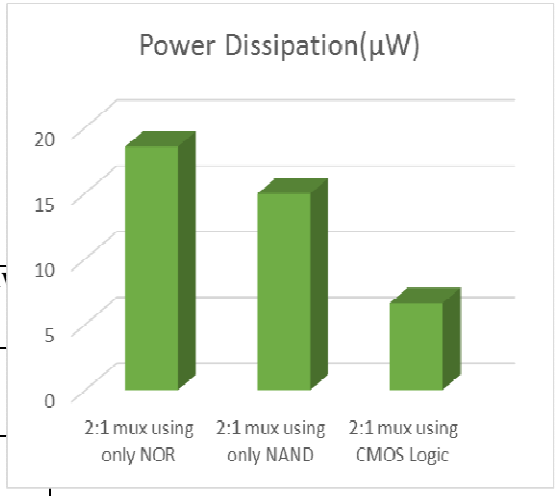


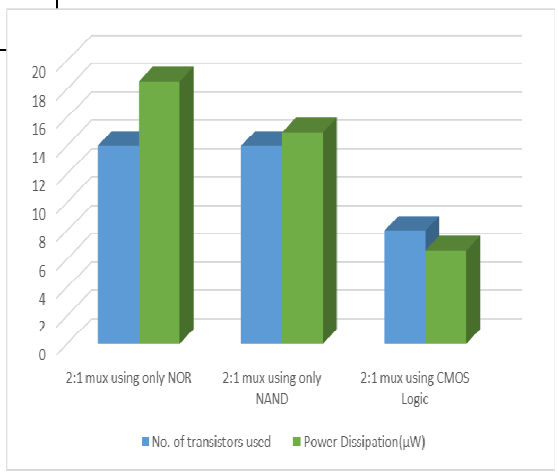
Fig.10 Timing diagram

V. COMPARATIVE STUDY

The main parameters taken into consideration are number of transistors used and the power dissipation of the 2:1 multiplexer circuit.

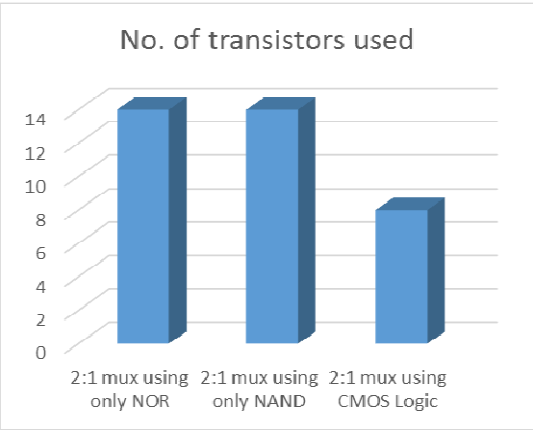
S.No	Name of the circuit	No. of transistors used	Power Dissipation(μ
1	2:1 mux using only NOR logic	14	18.53
2	2:1 mux using only NAND logic	14	14.939
3	2:1 mux using CMOS logic	8	6.6





VI. CONCLUSION

This analysis is made to propose the architecture of 2:1 multiplexer with two optimized goals. One is to enable a production with lesser transistors and the other is to reduce the power dissipation. As a result, it shows that CMOS logic is the better one to implement 2:1 mux when compared to NOR and NAND logic. Because the power dissipation is reduced to almost half than that of NOR and NAND logic. The power dissipation of CMOS logic is 94.9% less than the NOR logic and 77.4% less than that of NAND logic. The below given graphical representations show the comparison of number of transistors used and the corresponding power dissipation of all the three designs.



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