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LOW-POWER PULSE-TRIGGERED FLIP-FLOP DESIGN BASED ON A HIGH FREQUENCY VTCMOS SWITCHESACTIVE INDUCTOR

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***Abstract*--A power-gating scheme was presented to support multiple power-off modes and reduce the leakage power during short periods of inactivity. However, this scheme can suffer from high sensitivity to process variations, which impedes manufacturability. Recently, a new power-gating technique that is tolerant to process variations and scalable to more than two intermediate power-off modes. However this scheme can suffer from Increase in the lower threshold voltage, devices leads increased sub threshold leakage and hence more standby power consumption. A propose body biasing technique used to reduce the power. The proposed design requires less design effort and offers greater power reduction and smaller area cost than the previous method. In addition, it can be combined with existing techniques to offer further static power reduction benefits. Analysis and extensive simulation results demonstrate the effectiveness of the proposed design.**

I. INTRODUCTION

Many techniques have been presented in the literature for reducing static power. One common approach is to synthesize the circuit using dual-Vt libraries. High-Vt cells reduce the leakage current at the expense of reduced performance; thus their use on noncritical circuit domains reduces the leakage Power considerably without affecting circuit performance. Another technique exploits the fact that the leakage power consumed by each gate strongly depends on the input vector applied at the gate.

In order to reduce static power, it controls the input vector and the internal state of the circuit during periods of inactivity. Various techniques reduce peak rush current. A special class of these techniques reduces the large current rush by using one intermediate power off mode, while the methods presented in and apply a three step wakeup process. Intermediate power-off modes overcome another limitation of power switches the time required for recovering from the idle mode, referred to as the wake-up time.

Long wake-up time prohibits the use of power switches during short periods of inactivity In addition; there are applications that can exploit static power savings in parts of the system provided that these parts can wake up fast upon request. The long wake-up time of power switches prohibits their use in such cases too.

This technique requires that the memory elements are forced to specific logic values prior to the activation of a power-off mode. To address proposed a new flip-flop design to ensure that all internal gate nodes in the combinational logic will be forced to predictable states during the power-off mode.

II. LITERATURE SURVEY

ArchanaNagda and Rajendra Prasad, 2012

Exceeding Leakage power has become a major concern for the CMOS circuits in deep sub-micron process. As process moves to finer technologies, there is a decrease in the feature sizes and increase in the device density. Lowering the supply voltage leads to lower threshold voltages and oxide thickness.

High device density and low threshold voltages result in a significant increase in the leakage power dissipation. The main objective of this paper is to first extensively study the existing Leakage reduction techniques and compare them in terms of ability to reduce leakages and their associated delay overhead. In addition, several combinations of drain gating and power gating are discussed.

Carlos Ortega and Jonathan Tse, 2010

Power gating techniques are effective in mitigating leakage losses, which represent a significant portion of power consumption in nano scale circuits. We examine variants of two representative techniques, Cut-Off and Zigzag Cut-Off, and find that they offer an average of 80% and 20% in power savings, respectively, for asynchronous circuit families.

A new zero-delay wakeup technique for power gated asynchronous pipelines, which leverages the robustness of asynchronous circuits to delays and supply voltage variations. Our ZDRTO technique offers a tradeoff between wakeup time and static power reduction, making it suitable for power gating pipelines with low-duty cycle, busty usage patterns.

Dr. Neelam R. Prakash and Akash, 2013

A clock gating technique is presented for low power VLSI circuit design. Clock in digital circuits is used for synchronization of various components. Clock power is a major source of dynamic power consumed in synchronous circuits.

Clock-gating is a well-known technique to reduce clock power. In clock gating clock to an idle block is disabled. Thus significant amount of power consumption is reduced by employing clock gating. In this paper a 4-bit synchronous

counter is designed using clock gating.

Sandip B. Rahane and A.K. Kureshi, 2014

Leakage power reduction has become one of the top design priorities in battery operated ultra-low power circuits. Reduction in threshold voltage causes leakage power to increase exponentially.

Several techniques have been proposed that effectively minimize leakage power consumption. The most effective technique involves power gating in which a circuit is cut off from its power supply in sleep mode by means of a current switch. In this paper we present a review of conventional as well as emerging power gating schemes which are employed to reduce leakage power dissipation.

III. EXISTING SYSTEM

Description

The potential of active inductors has been often reduced by lack of accurate design methodologies and limitations due to the inherent noise sources. This paper deals with these two open issues for a high-frequency CMOS AI characterized by high-quality factor, low-power consumption, and low noise. First, it reports an effective design methodology for the implementation of high-frequency CMOS AIs with a high quality factor. In particular, it shows how, through an advanced small-signal circuit model, to carry out an accurate and reliable design at high frequency in modern nanoscale CMOS process. The design methodology is validated through cases of study at 13 GHz implemented in a standard 90-nm CMOS process and characterized experimentally. The results
show that the AI exhibits an equivalent inductance close to 3.2 nH with an associated quality factor close to 200. After, it reports a noise analysis. It shows that the AI exhibits a very low level of noise, enabling its application to the implementation of high-quality factor low-noise LC tank in high-frequency building blocks of radio frequency front-ends. The results show that the AI exhibits a noise power spectral density lower than −150 dBm/Hz.

Problem statement

To restore the virtual ground rail to its nominal value when the circuit transitions from the power-off mode to the active mode, the parasitic capacitance at the V_GND node has to be completely discharged through the power switches. However, the aggregate size of the power switches is not very large due to area constraints, while at the same time power switches are made of low-performing high-Vttransistors in order to minimize the leakage current.

The wakeup time is usually long relative to the circuit clock rate. This limits the applicability of this technique to idle periods that are longer than the wake-up time of the circuit. Consequently, the full leakage-savings potential of this architecture is not fully exploited.

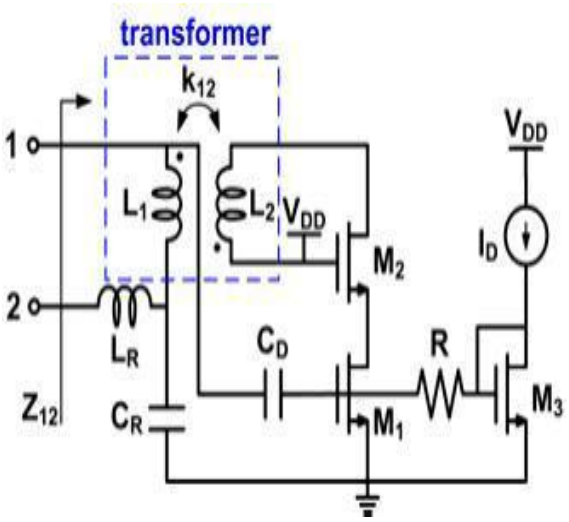
To overcome this limitation, the use of an intermediate power-off mode, where the virtual ground node is left charged to an intermediate voltage level. This is achieved through the use of a pMOS device connected in parallel with the nMOS footer. The pMOS is turned on in the intermediate power-off mode, and the virtual ground potential is adjusted to the threshold voltage of the pMOS.

The virtual ground node requires less time to discharge, although at the expense of less leakage reduction compared to the complete power-off mode. Even though they are very effective, these techniques cannot offer more than one intermediate power-off modes. For various applications on a 64-b Alpha processor, the use of two intermediate powergating modes offers further reduction in leakage of about 17% compared to single-mode gating.

Disadvantages

- The power-gating mechanism is more vulnerable to process variations due to the number of intermediate power-off modes.
- Reduction in multiplier and leakage current is very less.
- Only scalable upto two power off modes.

Existing circuit diagram



IV. PROPOSED SYSTEM

Description

The system consists of the main power switch transistor MP and two small transistors M0 and M1, each corresponding to an intermediate power-off mode. M0 corresponds to the dream mode and M1 corresponds to the sleep mode. Transistor MP is a high-Vt transistor and it remains on only during the active mode. Transistors M0 and M1 are small low-Vt transistors that are turned on only during the corresponding power-off mode. M0 is turned on during the dream mode and M1 is turned on during the sleep mode. Body biasing has been demonstrated to be effective in addressing process variability in a variety of simple chip designs.
However, for modern microprocessor ICs with multiple cores and dynamic voltage/frequency scaling , the use of body

biasing has significant implications. For a 16- core chip-multiprocessor implemented in a high-performance 22 nm technology, the body biases required to meet the frequency target at the lowest and highest voltage/frequency levels differ by an average of 0.7 V, implying that per-level biases are required to fully leverage body biasing.

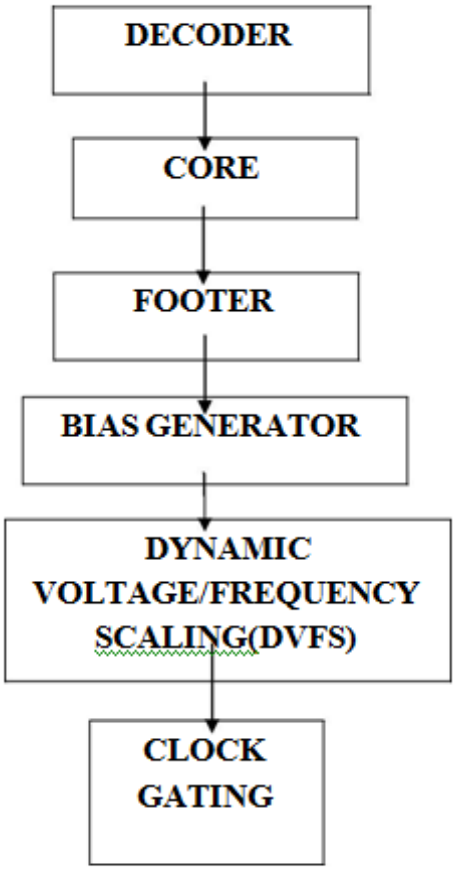
Advantages

The advantages of the proposed system are as follows:

- It consumes low static power.
- It has high tolerance to manufacturing process variations.

Ease of testability.

V. BLOCK DIAGRAM



WORKING PRINCIPLE

Body biasing has been demonstrated to be effective in addressing process variability in a variety of simple chip designs. While continuously adjusting the body biases during operation offers improvements in energy/efficiency, these benefits were outweighed by the implementation costs.

The implementation costs of continuously adjusting the body biases are dominated by the settling time of the controller. Existing controllers designed for simple general-purpose microprocessors do not optimize for settling time, and require D/A converters with high time constants.

A fully-analog controller that is able to achieve significantly lower settling time for a fixed area and power than previous controllers. With the proposed controller, continuously computing the body biases offers a better tradeoff in terms of area, performance, and power than computing unique body biases for each voltage/frequency level at chip power-on.

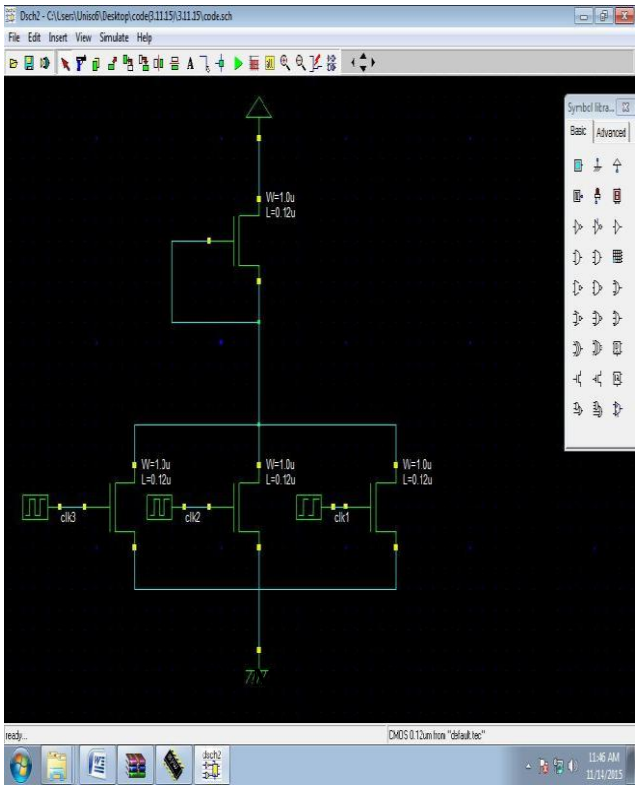
Further improvements in energy/efficiency can be achieved with an integrated approach to body biasing and DVFS. Because VDD is scaling and body biasing has different effects on static versus dynamic power, the operating point yielding the lowest overall power is dependent on the percentage of total power due to leakage. Leakage power, in turn, is strongly influenced by process variations.

EDA TOOLS

1. Simulation Tool : Model Sim –Altera 6.4a.
2. Language : VHDL
3. FPGA : XC3S1600E FPGA device for implementation

VI. RESULT ANALYSIS

VTCMOS OUTPUT ANALYSIS:



TOP 1 OUTPUT:

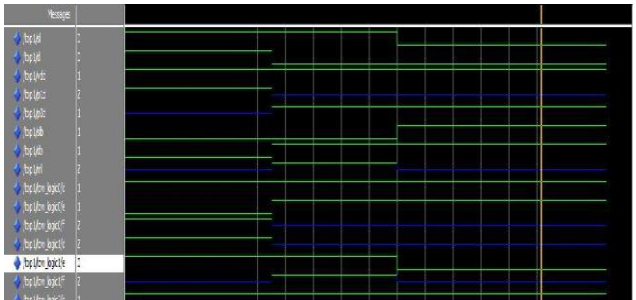
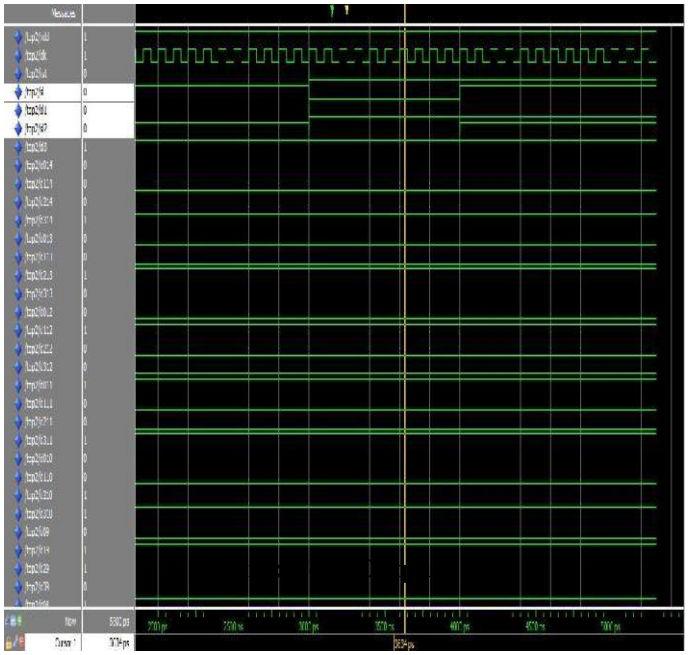


Fig: Top1 Output

TOP 2 OUTPUT:



VII. CONCLUSION

A Body biasing scheme that provides multiple power-off modes. The proposed design offered the advantage of simplicity and required minimum design effort. Extensive simulation results showed that, in contrast to a recent power-gating method, the proposed design is robust to process variations and it is scalable to more than two powers off modes.

The proposed scheme is based on clock gating technique. And gate based clock gating is used in design example. In conclusion clock gating technique significantly reduces dynamic power of sequential circuit, but may increase number of logics, and hence area will increase.

The technology is down scaling, the power dissipation in integrated circuit is more. Our aim is to reduce the maximum power without increasing delay and area. In the recent nano metre technologies, the leakage power is more than the dynamic. We are reducing the leakage power with the help of power gating techniques. This survey paper compares the differences in power gating techniques and its advantages. Moreover, it requires significantly less area and consumes much less power than the previous design. Finally, a reconfigurable version of this method can be used to increase the manufacturability and robustness of the proposed design in technologies with larger process variations.

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