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POWER AND BANDWIDTH SCALABLE 10-B 30-MS/S SAR ADC

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***Abstract*--Recently low power Analog to Digital Converters (ADCs) have been developed for many energy constrained applications such as wireless sensor networks and bio-medical applications. Successive approximation register (SAR) ADC are good candidates for low power applications and widely used for low energy application due to its minimum analog blocks. The static linearity performance in terms of the integral nonlinearity and differential nonlinearity and the parasitic effects of the split DAC, are analyzed. A code randomized calibration technique is done to correct the conversion nonlinearity in the conventional SAR ADC, which is verified by behavioral simulation. Here the SAR ADC is designed in such a way that the control module completely control the splitting up of modules and the speed of operation is changed using low level input bits. A dedicated multiplexer can be used to minimize the capacitor array structure. The control module controls the clock signal and determines the time at which the analog signal should enter the SAR logic. On attaining control over the time of arrival of input signals the speed of conversion can be increased and power utilization can be minimized.**

I. INTRODUCTION

Successive approximation registers Analog-to-digital converters are used as an alternative to the pipelined ADCs for battery-powered mobile applications, such as DVB-T, DVB-H and TDMB which require medium speed 10 MS/s–100 MS/s and medium-resolution. SAR ADCs achieve very low power consumption due to their simple structural design and operation. However, the SAR conversion relies basically on the arrangement of a capacitive DAC that subtracts the reference voltage from the input signal. The KT/C noise, capacitor mismatches, and parasitic of the split DAC affect the conversion precision. For medium resolution the KT/C noise requirement is satisfied with small capacitance, while other no idealities like parasitic and non linearity whose effect depends on the structure and the switching approach of the DAC, becomes significant. SAR ADCs uses Binary weighted capacitive DAC structure. But the capacitance of the DAC array increases exponentially with the resolution, which results in larger consumption of switching energy, area, and settling time. A valuable substitute for medium resolution is the split capacitive DAC. But it has the limitation that the parasitic capacitors destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity.

II. LITERATUTRE REVIEW

Chun-Cheng Liu and Soon-Jyh Chang, 2010

A 10-bit SAR ADC using a variable window function to reduce the unnecessary switching in DAC network. A differential architecture keeps the linearity error small up to the Nyquist frequency of sensor capacitance variation. Dual tail comparator is modified for low power and fast operations even in small supply voltages by adding few transistors, positive feedback during the regeneration is strengthened, and it results to reduce delay time in the layout simulation results by using CMOS technology analysis. At 10-MS/s and 1-V supply, the ADC consumes only 98μW and achieves an SNDR of 60.97 dB, resulting in an FOM of 11fJ/Conversion-step. The prototype is fabricated in a 0.18μm CMOS technology.

C.V. Shincy and K.Sivasankari, 2014

The comparator is one of the fundamental building block in ADC applications This paper presents based on comparator analysis in the ADC design to optimize power and area, maximize speed and clock frequency. According to an analytical expressions can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator is proposed in the circuit of a dual tail comparator. Dual tail comparator is modified for low power and fast operations even in small supply voltages by adding few transistors, positive feedback during the regeneration is strengthened, and it results to reduce delay time in the layout simulation results by using CMOS technology analysis.

Erkan Alpman and Hasnain Lakdawala, 2010

High-speed medium-resolution ADCs are widely utilized in high-speed communication systems, such as serial links, UWB, and OFDM-based 60GHz receivers. Due to complex DSP and low-power constraints, digital basebands are designed in low-leakage, high-VT low-power (LP) CMOS processes making the design of high-speed ADCs challenging. Time-Interleaved (TI) Successive Approximation Register-based (SAR) ADCs are ideally suited to these applications due to their highly scalable architecture and due to the steady improvement in matching and density of Metal-Finger Capacitors (MFC).

Mr. Jitendra Waghmare and Prof. P.M. Ghutke, 2014

The Design of analog to digital converter (ADC) for low power applications, so here is the selection of right architecture is very crucial. We have chosen successive approximation Analog to Digital Converter because of their

compact circuitry as compared with the Flash ADC which makes this SAR ADC inexpensive. Day By Day more and more applications are built on the basis of power consumption so this SAR ADC will be useful for high speed with medium resolution and low power consumption. The Successive Approximation (SAR) architecture is very suitable for data acquisition, it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 KHz to 50MHz.

III. EXISTING SYSTEM

The binary-weighted capacitive DAC is widely used in SAR ADCs. However the capacitance of the DAC array increases exponentially with the resolution, which imposes larger consumption of switching energy, area, and settling time. A valuable substitute is the split capacitive DAC, which has been recently reconsidered for medium resolution. Its key limitation lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity. However, by using the metal-insulator-metal (MIM) capacitor or/and DAC mismatch calibrations, the split structure can become suitable for a medium-resolution target. On the other hand, the conversion linearity is also directly correlated with the switching sequences of the DAC array where the conventional charge-redistribution switching results in worse conversion linearity and more energy losses. A V_{cm}-based switching technique has been recently proposed, which achieves a significant switching energy saving when compared with set-and-down and charge-recycling switching approaches.

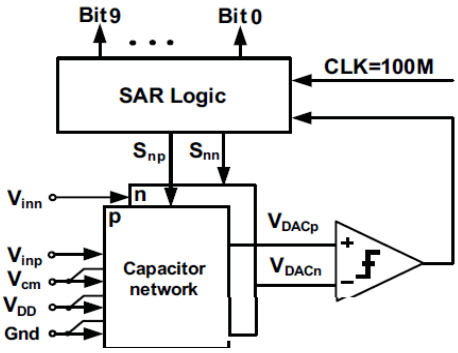

Fig.1 Block Diagram of ADC Architecture

IV. PROBLEM STATEMENT

When supply voltage is used as reference voltage the switching power becomes dynamic which is correlated with the switching sequence. The diagram represents a conventional single-ended *n*-bit split DAC structure. During the global sampling phase the input signal represented as V_{in} is stored in the entire capacitor array. The algorithmic conversion then starts by switching only the MSB capacitor to *V*DD and the others to Gnd. The comparator output predicts the switching logic for the MSB capacitor. If Out results low S_m, k is switched back to Gnd. If Out_ {comp} becomes high, then S_m,k maintained *V*DD. Simultaneously, the $S_{m,}$ k−1 switches to *V*DD for the next bit comparison. The above process repeats for $n - 1$ cycles. The conventional charge redistribution method is not effective in terms of power when discharging the MSB and charging the MSB/2 capacitor. The V_{cm} based switching method reduces the array capacitance to half resulting in 90% energy saving when compared with conventional method. The diagram represents the V_{cm} based switching algorithm. During the sampling phase voltage V_{in} gets stored in the capacitor array. During the conversion phase the bottom-plates of the capacitors gets switched to the V_{cm} first which raises the voltage −*V*in at the output.

DISADVANTAGE

The disadvantages of Split-SAR ADCs: Improved Linearity with Power and Speed Optimization are as follows:

- Superior conversion occurs due to the array's capacitors correlation during each bit cycling.
- Large switching transients are required which leads to insufficient DAC settling and supply ripples.
- Delay due to V_{cm}-based switching in DAC.

V. PROPOSED SYSTEM

DESCRIPTION OF PROPOSED SYSTEM

A/D conversion is obtained with many algorithms. For obtaining power effectiveness, what often matters is not inventing new methods but finding the best use of known algorithms and achieving the optimum for the foreseen technology and the given specifications. High speed and medium-to-high resolution normally call for pipeline, two-step, or sub ranging schemes. The basic building blocks are the track-and hold, the comparator, and the op-amp. With medium resolution, the input track and hold is a source follower with passive sampling. Clock feed through is minimized with dummy elements and body effect is cancelled out by connecting the source and substrate. The power depends on the capacitive load that, in turn, is proportional to the number, N, of comparators served by the T&H. Since gm/CL is the relevant parameter power increases with the square of N. The power of the comparator depends on the resolution. For several tens of mV, just a latch makes the comparator. For resolutions from ten to few tens of mV, however, it is necessary to use a simple preamplifier before the latch.

ADVANTAGE

The advantages of the proposed system are as follows:

- It eliminates the errors and conventional switching.

- The reduction of switching power as well as the digital power from switching buffers.
- High accuracy.

PROPOSED SYSTEM ARCHITECTURE CONFIGURABLE SPLIT SAR ADC

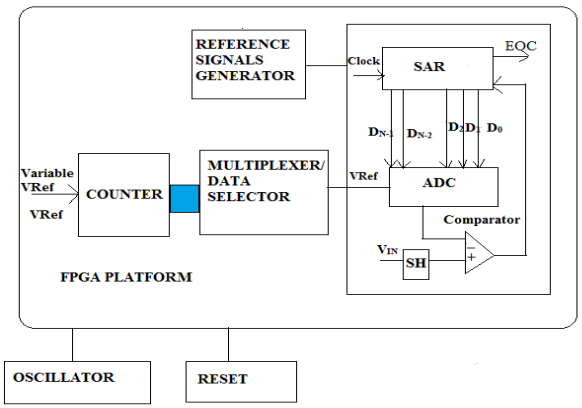

Fig.2 Split SAR ADC- Functional Block Diagram

VI. FUNCTIONAL BLOCK DIAGRAM

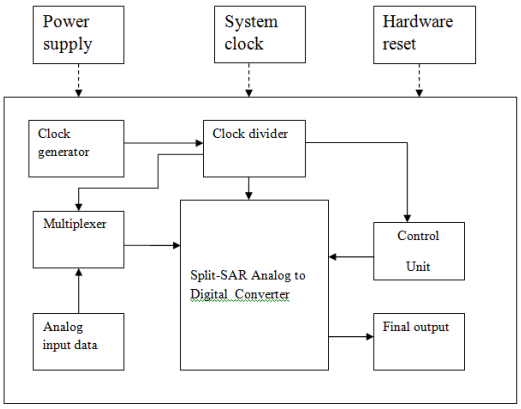

Fig.2 Functional Diagram of Proposed system

BLOCK DESCRIPTION OF PROPOSED SYSTEM

In the proposed system we are planning to implement SAR ADC in a configurable manner with different frequency inputs, the configurable means that the entire ADC architecture can work with different perfromance by changing the Vref of the ADC. Normally in all ADC Vref , Vin , Vth plays a major role in adc conversion by varying the values of Vref we can change the performance of the ADC.

SAR ADCs provide a high degree of configurability on both circuit level and architectural level. At architectural level the loop order and oversampling ratio can be changed, the number of included blocks, and way these blocks are arranged. At circuit level many things could change, such as bias currents, amplifier performance, quantizer resolution etc.

If an ADC is reconfigured in the way the blocks in the ADC are used and ordered, it is an architectural change of the ADC, or architectural reconfigurability. These blocks can also be changed, for instance how the amplifiers are biased, or how many bits of resolution that a quantizer has in a SAR ADC. These are examples of how circuit level reconfigurability is applied to an ADC.

VII. RESULT ANALYSIS

ASIG OUTPUT

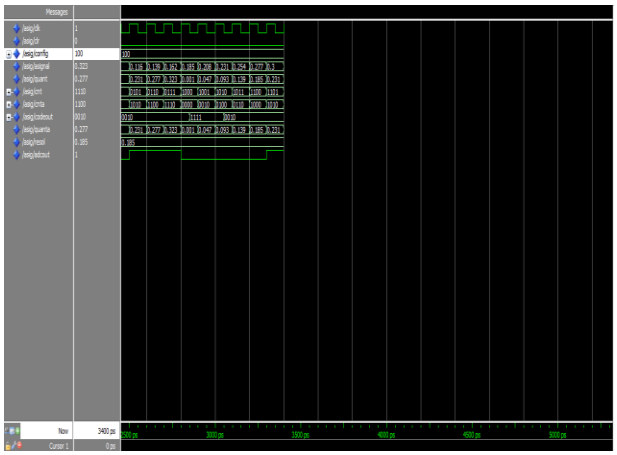

Fig.ASIG Output

APPLICATION OF SONDAE OUTPUT

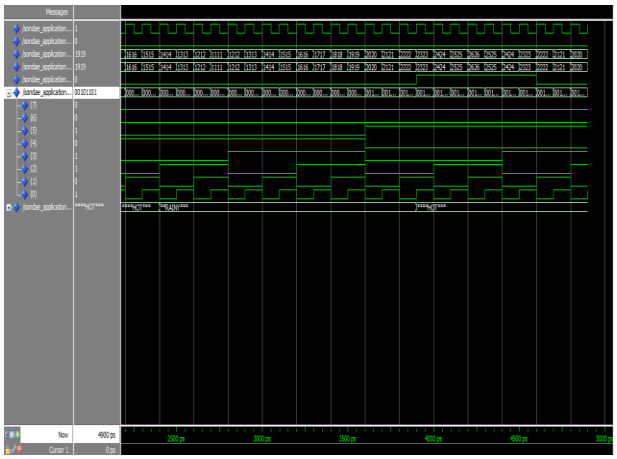

Fig.Application of SONDAE

INTEGRATION OUTPUT

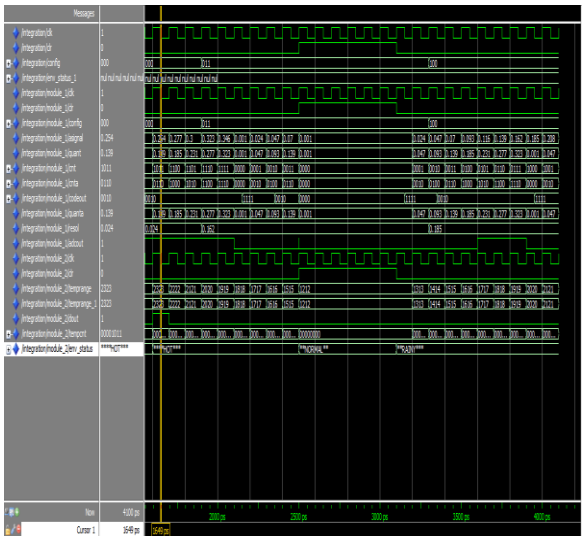

Fig.Integration Output

VIII. CONCLUSION

Two 1.2 V 10-b SAR ADCs operating at tens of MS/s with additional multiplexer was presented. The linearity behaviors of the DACs switching and structure were analyzed and verified by both simulated and measured results. According to an analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator is proposed in the circuit of a dual tail comparator. It has been designed adopting a binary weighted with attenuation capacitor array featuring a linearity and a total capacitance similar to a conventional binary weighted array but without requiring critical full-custom sub fF capacitors. The design and the layout of the array have been accurately optimized in order to reduce the parasitic capacitances at the top-plate node of the sub-DAC which degrade the linearity. This switching technique provides superior conversion linearity when compared with the conventional method because of its array's capacitors correlation during each bit cycling. The proposed code randomized calibration can eliminate the large DNL and INL errors during switching. Measured results demonstrated that both higher speed and lower power is achieved by using proposed SAR ADC architecture.

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