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Performance and analysis of Stacked Nanosheets Gate All Around Thin Film Transistor for Different Dielectric Materials

CH. Haveesh Kumar Reddy[#1], CH. Avinash[#2], S Satyanand[#3], Jenyfal Sampson[*4]

[#] *Electronics and communication engineering,Kalasalingam academy of research and education, Krishnankovil, India*

[*] *Electronics and communication engineering,Kalasalingam academy of research and education, Krishnankovil, India*

***Abstract*— The Gate All Around Thin Film Transistor (TFT) with two stacked nano sheets is formed in TCAD with the gate length of 1um. The Ion/Ioff is calculated for TFT with different dielectric materials and the IV characteristics have been plotted for different work functions to ensure the material for SOP (System on Panel) Applications. To design a Stacked Nanosheet Gate-All-Around Thin-Film-Transistor (SNS-GAA) by using silicon as the channel material and SiO2 as the Gate Oxide material. To calculate the performance of multiple materials by comparing the performance of the SNS-GAA-TFT by using different type of channel and oxide materials. Comparing the performance of transistors with different materials. To ensure that which material provides better performance.**

***Index Terms*—About four key words or phrases in alphabetical order, separated by commas.**

I. Introduction

In recent years smart phones displays are fabricated with AMOLED displays because of better viewing experience and the Transistor which is used in AMOLED displays are Thin Film Transistor (TFT). Since it has low thickness short channel effects (SCE) and Leakage current have been reduced. Gate all around structure reduces leakage current and gate completely takes control over the channel. [1] showed the Thin Film Transistor gives the better performance when Gate All Around is used. Dielectric material also one of the important elements to increase the performance of the device. High-k dielectric materials having high permittivity which is reduced the leakage current [2]. Thin Film Transistor mainly suits for AMOLED applications and high driving current applications. Thin Film Transistor performance can be increased by replacing a channel material and an oxide material. In this work, the performance has been calibrated for different dielectric materials. Hafnium dioxide (HfO_2) is a high-k dielectric which has bandgap of 5.3 to 5.7 eV, and it has high permittivity. The dielectric constant of HfO_2 is higher than normal dielectrics [2]. Gallium oxide (Ga_2O_3) has a bandgap of 4.5 to 4.9 eV, and which is widely used in optoelectronics [3]. Germanium dioxide (GeO_2) has a refractive index of 1.7 and it has a good optical dispersion property which made GeO_2 is widely used in optical applications [4]. First the p-channel Gate All Around Thin Film Transistor is formed in Technology Computer-Aided Design (TCAD) by using the details from Table I which have been taken from [1]. Once the IV characteristics matches with the experimental results [1], the same device simulated with different dielectric materials. Drift Diffusion model and Shockley-Read-Hall Recombination (SRH) are used to calibrate the results in TCAD. The multi-gate structure, in tri-gate [5], and gate-all-around [6], [7] with ultra-thin body channel [8], [9],effectively increase the gate control of the channel and thus reduce short channel effect (SCE) and leakage current. In recent studies [10], [11] have used 3D stacking technologies to integrate with tri-gate and gate-all-around which are multi-gate structures. However, the nanosheet channel of multi-gate TFT has ultranarrow thickness yields a low conducting area and also has a high parasitic S/D resistance, resulting in the low driving current. Therefore, we provide a horizontally p-type multi-layer stacked nanosheets thin-film transistor with the gate-all-around structure to overcome this low driving current issue.

II. EXPERIMENT DETAILS

The structure of the device in the Fig.1, Fig.2 and Fig.3 has been formed in the TCAD with the details given in the Table I [3]. The work function is 4.725 has been used for the simulation and the direct metal gate has been given as a contact in TCAD. [3] structure has been formed by using SiO_2 material. But when the device will be scaled down High-k dielectrics will be useful to control leakage current and Improve the performance. So, the device has been simulated with different materials and the performance has been analyzed. The IV Characteristics have been taken for the device (Gate All Around Thin Film Transistor Stacked Nanosheets) for the values V_{GS}= -1V and V_{DS} = -1V with different materials like SiO_2, Ga_2O_3, HfO_2, GeO_2. Fig.4(a) transfer characteristics clearly shows the better performance of the material among them, based on the Ion/Ioff calculation. Fig 4 output characteristics have been made for the same different materials.

Based on the output results, High-k dielectrics increased the performance of the Thin Film Transistor and simultaneously Gate all around structure reduces the leakage current and Short channel effects which can apply for AMOLED applications.

*A. **Drift-Diffusion Model:***

In drift-diffusion model, the electron current density is:

$$\vec{J_n} = \mu_n(n\nabla E_C - 1.5nkT\nabla ln m_n) + D_n(\nabla_n - n\nabla ln\gamma_n)$$

and the current density of holes is given by:

$$\vec{J_p} = \mu_p(p\nabla E_v - 1.5pkT\nabla ln m_p) + D_p(\nabla_p - n\nabla ln\gamma_p)$$

The first term considers the contribution due to the spatial variations of the electrostatic potential, the electron affinity, and the band gap. The remaining terms consider the contribution due to the gradient of concentration, and the spatial variation of the effective masses m_n and m_p. Through the Einstein relation the diffusivities are derived using the mobilities [8].

$$D_n = kT\mu_n and D_p = kT\mu_p$$

*B. **Shockley-Read-Hall Recombination***

Recombination through deep defect levels in the gap is usually labeled SRH recombination. In Sentaurus device,the following form is implemented:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)}$$

With: $n_1 = n_{i,eff}\exp\left(\frac{E_{trap}}{KT}\right)$

$$p_1 = n_{i,eff}\exp\left(\frac{-E_{trap}}{KT}\right)$$

Where E_{trap} is the difference between the defect level and intrinsic level. The variable E_{trap} is accessible in the parameter file. The Silicon default value is E_{trap} =0.

The doping dependence of the SRH lifetimes is modeled in Sentaurus device by use of the Scharfetter relation: [8].

$$\tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{dop} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}}$$

The fabrication steps clearly explained in [1] like the dual-channel SNS-GAATFT is manufactured on the 6-inch silicon wafer by first rising a 400-nm thermal SiO_2 layer. A 50 nm thick undoped amorphous silicon (a-Si) layer was deposited as the bottom channel at 550°C by low-pressure chemical vapor deposition (LPCVD). Then, the a-Si layer was crystallized at 600°C for 24 hours in an ambient nitrogen atmosphere using a solid-phase recrystallization (SPC) method, forming large grains. A dry oxide 30 nm thick has been developed to separate two vertically stacked channels. Then, LPCVD deposited another 50-nm-thick a-Si and used SPC as the top stream. The oxidation trimming process used by the top channel to form a nanosheet (NS). Electron beam lithography (EBL) patterned the active region of the system and transferred by reactive ion etching (RIE). The devices are dipped into BOE solution for suspending nanosheets to form GAA structure. . Next, as the gate oxide layer, a 10-nm thermal SiO2 layer was developed. Then, as a gate electrode, 200-nm-thick in-situ doped n+ poly-Si was created, then patterned by EBL and RIE. Both the bottom and top channels were injected with the same 5E15 dose of BF2 ions with 90 keV and 30 keV, respectively. Then, the rapid thermal annealing (RTA) triggered the dopant. The top and bottom regions of the channel are doped with the same concentration after RTA. Secondary ion mass spectrometer (SIMS) confirms the concentration of the top and the bottom channel region. As a passivation layer a 200-nm-thick TEOS was deposited. Eventually, a metallization of 300-nm-thick Al-Si-Cu was performed and sintered for 30 minutes at 400°C.

Table I

S.No	Parameters	Values(unit)
1	Gate length, L_G	1000(nm)
2	Channel fin width, F_W	80(nm)
3	Top channel fin height, F_{ht}	20(nm)
4	Bottom channel fin height, F_{hb}	20(nm)
5	Interlayer oxide	15(nm)
6	Gate oxide	10(nm)
7	S/D doping (Boron)	$1x10^{20}$(nm)
8	Channel doping (Phosphorous)	$1x10^{16}$(nm)

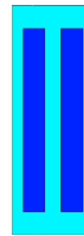

Fig. 1 Oxide Layer around channels

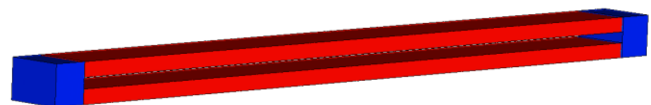

Fig. 2 Stacked Nanosheets without oxide layer

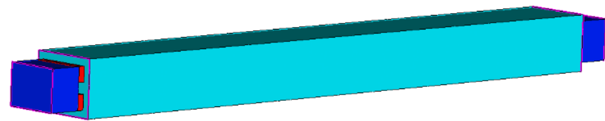

Fig. 3 Gate All Around Stacked Nano sheet

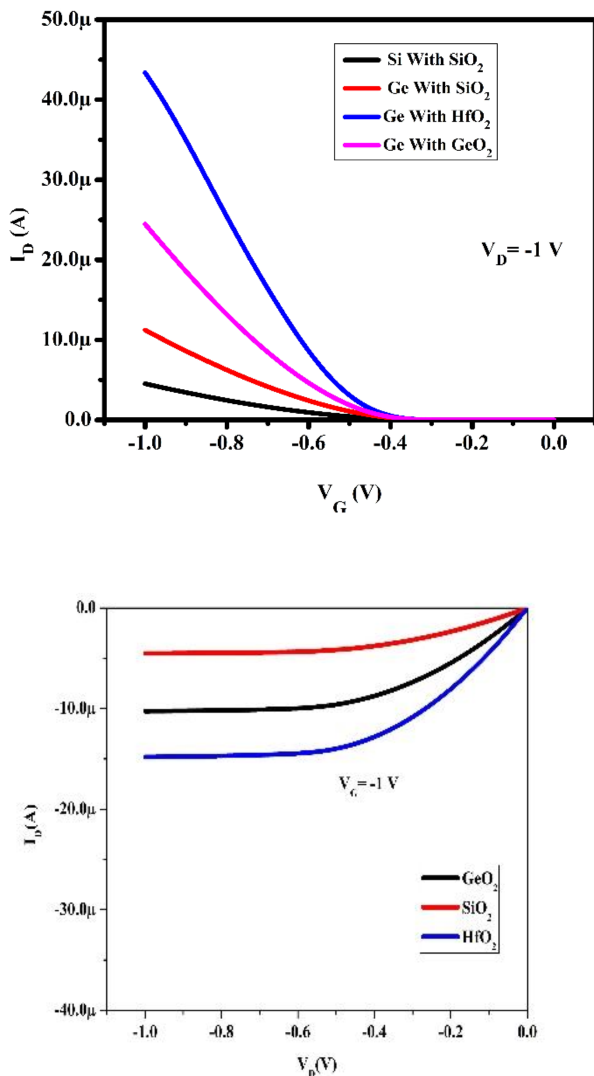

Fig. 4 IV Characteristics of Gate All Around Stacked Nanosheet with different dielectric material

III. RESULTS AND DISCUSSION

Filter TFT Simple or Stacked Nanosheets The above study initially contrasted simple-NS and JL-based stacks of NS. The uniform ID – VG distributions of JL-TFTs with simple-NS and stacked-NS are shown. Both ID / VG functions have been multiplied for each instrument's entire transversal size.

Rising nanosheet was about 110 and 100 nm, accordingly, throughout the top length of the simple- NS and packed-NS modules. Throughout the simple-ns and stacked-ns the scales subthreshold (SS).

IV. CONCLUSION

The simple handling and efficiency, improved performance of the above GAA JL-TFT stacked NS outlets were indicated. With that of the duration and temperature of the gate, the stacked NS GAA JL-TFTs displayed fewer variability. Ultimately, JL-TFT stacked-NS has the opportunity to be used in new technology clusters in 3D stacked optimized-circuit programs.

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