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RECONFIGURABLE SWITCHING PATTERN FOR SELECTIVE HARMONIC ELIMINATION IN CASCADED MULTILEVEL INVERTER USING FPGA

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***Abstract*: This paper aims to maintain the degree of freedom even when the modulation index reduces so that harmonics can be controlled. In order to achieve the degree of freedom constant reconfigurable selective harmonic elimination technique is been proposed in place of traditional selective harmonic elimination technique so that even when the modulation index reduces degree of freedom is been maintained as far to control the harmonics. Here field programmable gate array chip is been coded in order to visualize various output levels. This proposed scheme deals with reducing the selective harmonic elimination in cascaded multilevel inverter using Field Programming Gate Array (FPGA). Single phase inverter is been designed in which even harmonics is been eliminated due to quarter wave symmetry. As triplen harmonics are been present in single phase inverter it should be controlled. The traditional model involves selective harmonic elimination technique which is been suited for the modulation index from 1 to 0.5. Below 0.5 the switching angles converge to 90 degree in which it is difficult to maintain the degree of harmonics and hence harmonics cannot be controlled. In order to avoid those problems, reconfigurable selective harmonic technique is been proposed in which degree of freedom is been maintained even when the modulation index reduces from 0.5. This technique is been implemented for controlling the harmonics at symmetrical voltage levels.**

***Index Terms*—voltage and current THD, multilevel inverter.**

I. INTRODUCTION

Inverter is a power electronic device that converts the Direct Current (DC) into Alternating Current (AC). The harmonics can be present in any system where inverters are used. The main aim of using an inverter is to produce an ac output from the dc source. It is used in medium voltage applications, uninterruptable power supply and Flexible AC Transmission Systems.The effect of harmonics will be a serious case affecting the sensitive equipment, improper zero crossing detection and miss operation of the equipment. In single phase inverter even order harmonics are absent in the output waveform of inverter as it has quarter wave symmetry and the triplen harmonics are automatically cancelled in a balanced three phase system. Harmonic in a device has a serious effect to the sensitive equipment and it is need to implement different modulation schemes in order to improve the harmonic reduction.

A. MULTILEVEL INVERTER

Multilevel inverters are in favor of academic as well as industry in the recent decade for both high power and medium power applications. In addition they can synthesize switched waveforms with lower levels of harmonic distortion compared to a two level converter. Multilevel converters have received increased interest recently as a result of their ability to generate high quality output waveforms with a low switching frequency. The multilevel concept is used to decrease the harmonic distortion in the output waveform without increasing the inverter power output. Multilevel inverter has aroused a great emerge in reducing the harmonics.

B.SURVEY OF CASCADED MULTILEVEL INVERTER

Cascaded multilevel inverters synthesize a medium voltage output based on a series connection of power cells which use standard low voltage component configurations. This characteristic allows one to achieve high quality output voltages and input current due to their intrinsic component redundancy.

Due to these features, it recognized as an important alternative in the medium voltage inverter market. It presents a survey of different topologies, control strategies and modulation techniques used by the inverters. Regenerative and advanced topologies are also included.

C. PROPOSED SYSTEM

The proposed scheme deals with reducing the selective harmonics in cascaded multilevel inverter using Field Programming Gate Array(FPGA). Single phase inverter is been designed in which even order harmonics has been eliminated due to quarter wave symmetry.

The traditional model involves selective harmonic elimination technique which is been suited for the modulation index from 1 to 0.5. Below 0.5 the switching angles converge to 90 degree in which it is difficult to maintain the degree of harmonics and hence harmonics cannot be controlled.

In order to avoid those problems, reconfigurable selective harmonic technique is been proposed in which degree of freedom is been maintained even when the modulation index reduces from 0.5. This technique is been implemented for controlling the harmonics at symmetrical voltage levels.

II. OBJECTIVE

The main objective of the proposed system is to maintain the degree of freedom even when the modulation index reduces so that harmonics can be controlled. Traditional SHE PWM technique meets the problem when modulation index reduces <0.5, so that degree of freedom cannot be maintained so harmonics cannot be controlled. In order to achieve the degree of freedom constant reconfigurable traditional selective harmonic elimination technique so that even when the modulation index reduces degree of freedom is been maintained as far to control the harmonic.

III. CIRCUIT DIAGRAM

The circuit diagram for seven level cascaded multilevel inverter is given in the figure 2. It consists of Three H Bridge circuit with symmetric voltage. The positive voltage +vdc is obtained by switching on sa1 and sa2 switches and the upper leg is switched on for the remaining H bridge circuits to obtain the positive voltage. The same procedure is applied for the negative voltage where sa3 and sa4 switches is been turned on and lower leg switches is switched on for the remaining H bridges.

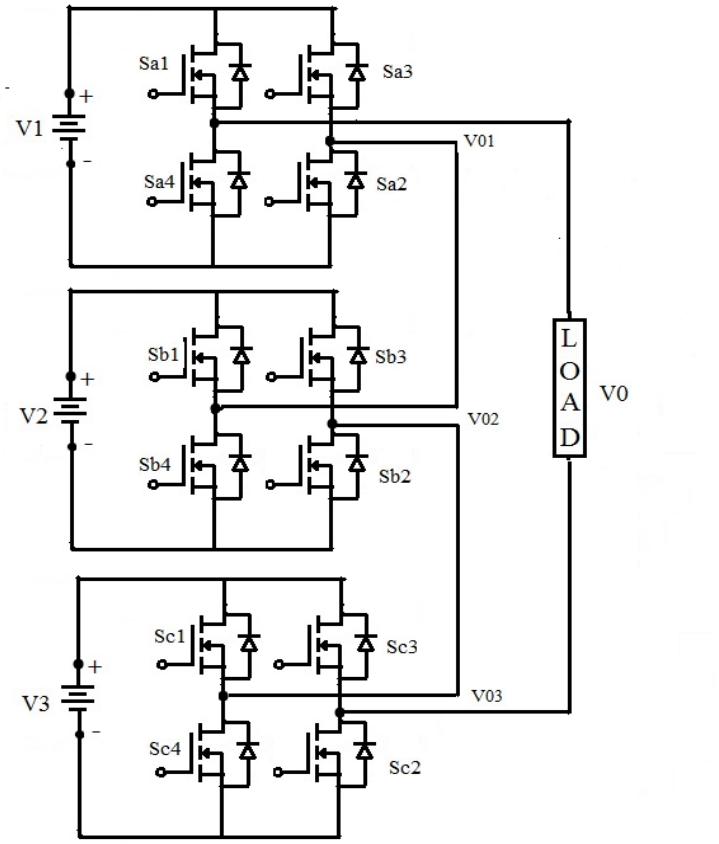


Fig 1 CASCADED MULTILEVELINVERTER

Table 1. SWITCHING WAVEFORMS

D1	D2	D3	D1	D2	D3	SWITCHING WAVEFORM
0	0	0	-	-	-	
0	0	1	-	-	+	
0	1	0	-	+	-	
0	1	1	-	+	+	
1	0	0	+	-	-	
1	0	1	+	-	+	
1	1	0	+	+	-	
1	1	1	+	+	+	

Table 2. VALID AND INVALID WAVEFORMS

Sector	Combinations	Edges
Valid states	111 110 101	+ ++ + + - + - +
Invalid states	000 001 010 011 100	- - - - - + - + - - + + + - -

IV. BLOCK DIAGRAM

The very high level integrated circuit hardware description language (VHDL) coding is burn in FPGA chip. The hardware kit consist of various Switches in which we can burn the required program Multilevel inverter produce common bus voltage so that it reduces the stress of the motor and prevent the motor from being damage. VHDL coding can store several coding according to the requirement of the switches. The final output is been noted in CRO and power logger to verify the THD acquired for the given

switching angle.

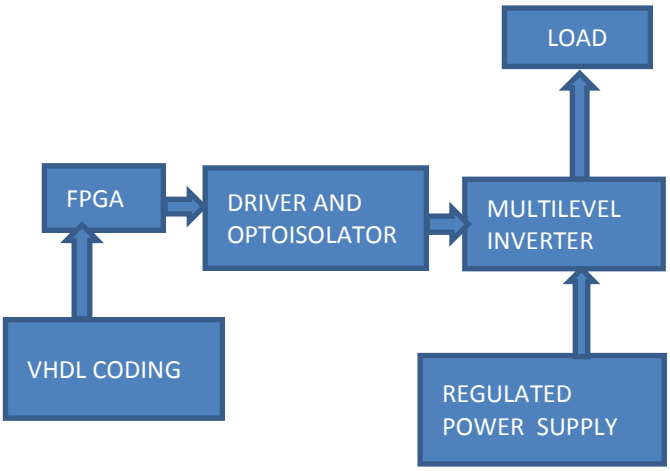


Fig 1. BLOCK DIAGRAM

A. PSO ALGORITHM

PSO is a computational method that optimize a problem by iteratively trying to improve the candidate solution with regard to a given measure of quality. Each particle movement is influenced by its local best known position and also guided towards the best known position in the search space.. The best position of particle obtained so far is termed as personal best (P_{best}) and the best position in the entire region of swarm is called global best (G_{best}). An inertia weight (w) controls the velocity of the movement of the particles.

The velocity of this updated by

$$vit+1=wvit+c1r1(Pbesti-xit)+c2r2(Gbesti-xit)$$

The individual positions are updated by $x_i^{t+1} = x_i^t + v_i^{t+1}$

Where

w be the inertia weight, X and v be the position and velocity of the ith particle P_{best} be the best position found by the personal best and G_{best} be the best position found by the global best. r1, r2 be random values uniformly distributed within [0, 1]

B. PROPOSED RECONFIGURABLE SHE-PWM TECHNIQUE CALCULATION

There are two ways of identifying the possibility of valid states and invalid states. The frequent falling edge result in negative wave so it is not possible to construct a wave and for a seven level CMLI most of the switching angles should be at rising edges, so that it is feasible to construct a wave for the given switching angles

Table 2. various switching angles

θ1	**θ2**	**θ3**	**THD %**
10.13	31.20	58.91	52.50
11.68	31.19	58.58	52.37
10.71	37.07	69.93	42.55
19.32	66.12	80.15	33.74

C. STEPS TO FIND MINIMUM OBJECTIVE FUNCTION

- Switching angles are been generated randomly.
- Substitute those switching angles in Fourier analysis.

Vhn= 4vdc/nπ[cosΘ1 +cosΘ2 +cosΘ3] for MI = 0.67 to 01

Vhn= 4vdc/nπ[cosΘ1 +cosΘ2 -cosΘ3] for MI =0.34 to 0.66

Vhn= 4vdc/nπ[cosΘ1 -cosΘ2 +cosΘ3] for MI =0.01 to 0.33

- From the above find h1,h3 and h5.
- Find the objective function.

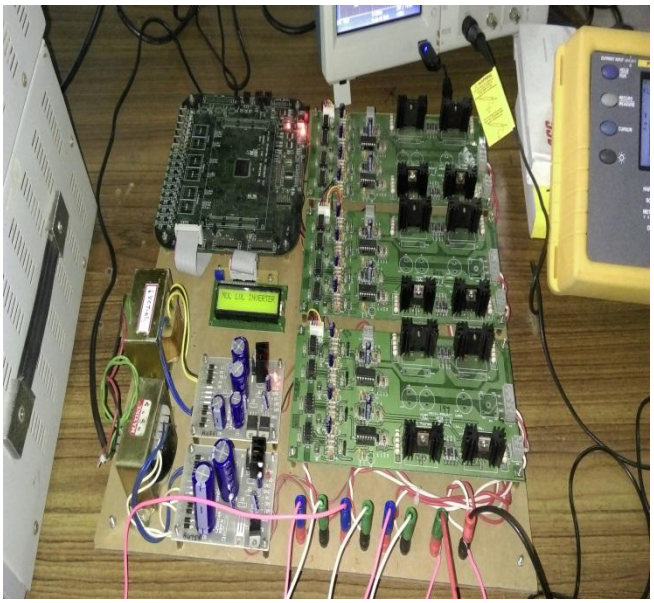
$$f_{SHE-PWM} = \min\left\{\left(100\frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{n=5,}^{7}\frac{1}{n}\left(50\frac{V_{hn}}{V_1}\right)^2\right\}$$

- Repeat the above steps to get the minimum objective function

D. FIELD PROGRAMMING GATE ARRAY (FGPA)

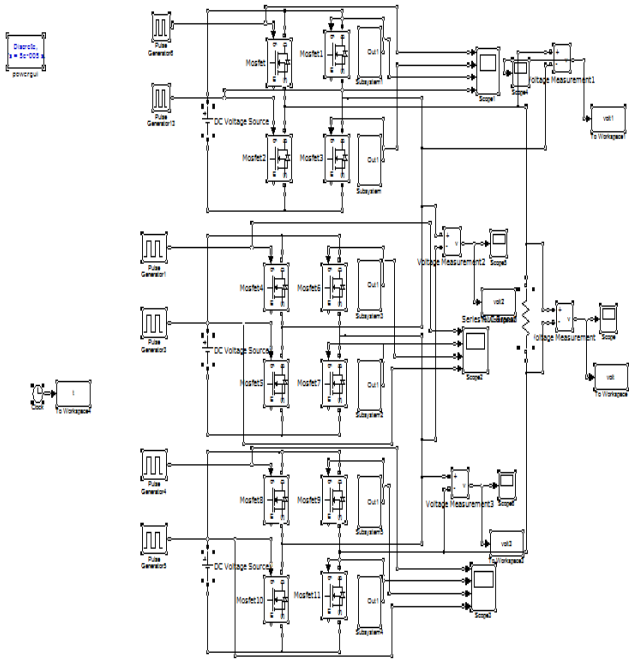
Field Programming Gate Array is the function of configurable building blocks that can be reprogrammed to several times according to the specific applications after manufactured. It is a chip made up of configurable building blocks that can be re programmed up to a number of times according to the voltage levels. The program can be dumped into a chip by very high level integrated circuit hardware description language coding. The FPGA chip is being preferred for this type due to its high computational speed. The total harmonic distortion for various switching angles is been calculated and is been coded in VHDL by Xilinx software and the output is been observed by running the constructed program in that Xilinx software. There are three types of VHDL coding listed as

- Behavioural(process() clk)
- Structural(hardware description)
- Data flow(Boolean equation)



V. SIMULATION CIRCUIT

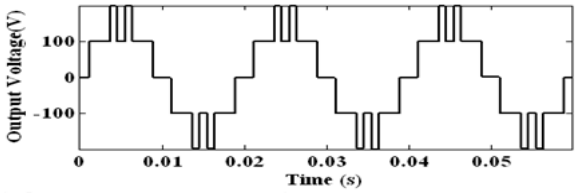
A. MODELLING OF SEVEN LEVEL INVERTER

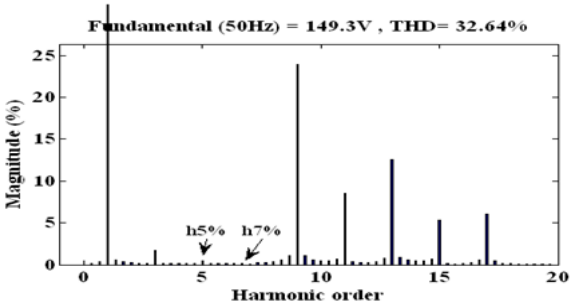


B. SIMULATION PROGRAM

```
A=[19.32695 66.12537 80.15957];
A1=A(1);
A2=A(2);
A3=A(3);
D1=A1*(0.01/180);
D2=A2*(0.01/180);
D3=A3*(0.01/180);
D4=0.01-D3;
D5=0.01-D2;
D6=0.01-D1;
D7=0.01+D1;
D8=0.01+D2;
D9=0.01+D3;
D10=0.02-D3;
D11=0.02-D2;
D12=0.02-D1;
PWA11=((0.01-0)*(100/0.02));
PWA21=((D6-D1)*(100/0.02));
PWA22=((D7-0.01)*(100/0.02));
PWA23=((0.02-D12)*(100/0.02));
PWA31=((D1-0)*(100/0.02));
PWA32=((0.01-D6)*(100/0.02));
PWA33=((D12-D7)*(100/0.02));
PWA41=((0.02-0.01)*(100/0.02));
PWB11=((0.01-0)*(100/0.02));
PWB21=((D3-D2)*(100/0.02));
PWB22=((D8-0.01)*(100/0.02));
PWB23=((0.02-D9)*(100/0.02));
PWB31=((D2-0)*(100/0.02));
PWB32=((0.01-D3)*(100/0.02));
PWB33=((D9-D8)*(100/0.02));
PWB41=((0.02-0.01)*(100/0.02));
PWC11=((0.01-0)*(100/0.02));
PWC21=((D5-D4)*(100/0.02));
PWC22=((D10-0.01)*(100/0.02));
PWC23=((0.02-D11)*(100/0.02));
PWC31=((D4-0)*(100/0.02));
PWC32=((0.01-D5)*(100/0.02));
PWC33=((D11-D10)*(100/0.02));
PWC41=((0.02-0.01)*(100/0.02));
```

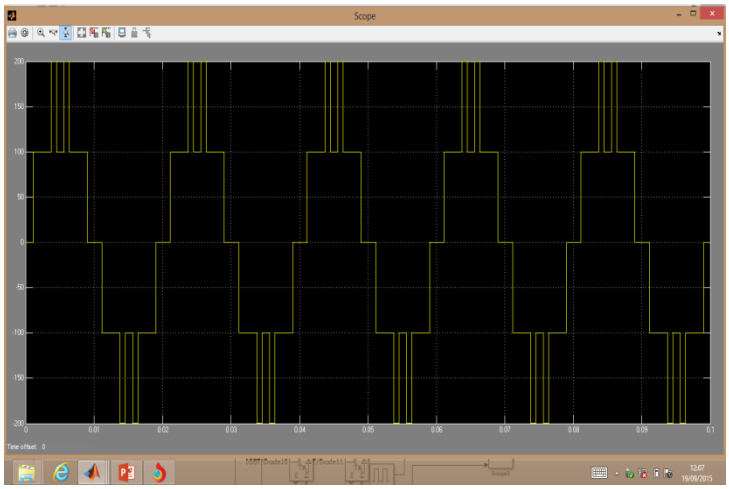
C. WAVEFORM FOR SYMMETRIC RECONFIGURABLE SWITCHING PATTERN





D. CALCULATIONS

Let us assume for the given pulse width,
Upper bound=0.01 and
Lower bound=0
Then the pulse width= ((0.01-0)/0.02)x100
Pulse width=50
As there is no delay in the given pulse width, Delay=0
Width is calculated to substitute them in VHDL coding,
T = 1/100
F =100
Width= 20000000/100=200000 count
Delay=0
Therefore the switch will be ON at 0 to 200000 count.



VI. CONCLUSION

Thus the output for reconfigurable selective harmonic elimination technique in cascaded multilevel inverter is been analyzed using various switching angles by FPGA. It is been clearly observed that it is no effect on the degree of freedom when the modulation index reduces. It plays an important role in order to control the harmonics. The output for the minimum THD value is been calculated and FFT analysis is been taken for the required switching pattern.

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