International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)
ISSN: 0976-1353 Volume 8 Issue 1 –APRIL 2014.

COMPREHENSIVE ANALYSIS OF ENHANCED CARRY-LOOK AHEAD ADDER USING DIFFERENT LOGIC STYLES

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***Abstract*--- An Adder is a basic component in a central processing unit. A carry look-ahead adder improves speed by reducing the amount of time required to resolve the carry bits. In this paper 4-bit CLA has been designed using various logic styles such as Standard CMOS, DCVS,Pseudo NMOS, PTL and Domino logic style. Performance of CLA is measured by comparing the results in terms ofpropagation delay, average power dissipation and power delay product. The paper also includes the design of a modified carry look-ahead adder which based on the analysis can be regarded faster the carry look-ahead adder.**

***Index Terms*— Carry look ahead adder, DCVS, Domino, MCLA, Pseudo, PTL and Standard CMOS logic.**

I. INTRODUCTION

High performance data path circuits continue to be a topic of interest as technologies are scaled to nanometer [1]. Adders fall under this group. Adders are logic circuits designed to perform high speed arithmetic operations and are important in digital systems because of their intensive use in basic operations such as subtraction, multiplication and division [2]. It is widely used in generic computer [3] because it is very important for adding data in the processor. The speed of execution is the most important factor that needs to be considered for appraising the quality of an adder. CLA is an important building block for digital circuit. It is constructed using XOR, AND and OR gates. The Carry Look Ahead Adder is able to generate carries before the sum is produced using the propage and generate logic to make addition much faster. In the paper, CLA is implemented using various logic styles such as Standard CMOS, DCVS, Pseudo, PTL and Domino logic style. Tanner simulation has been done for 0.25um to determine Propagation Delay, Average Power Consumption, and Power Delay Product (PDP).The rest of the paper is organized as follows. Section II describes the block diagram and basic construction of CLA. The design methodology of CLA using different logic style is described in section III. Different parameters are discussed in section IV. Results and analysis is done in section V. The paper is concluded in section VI.

II. OVERVIEW OF CLA

The basic design structure of CLA is discussed in this section. 4-bit CLA is designed using 4 1-bit full adders. The carry-look-ahead adder logic uses concept of generating and propagating the carry bit. Figure 1 demonstrates a 4-bit CLA. Let i be the index of stage. There are 3 inputs A_i and B_i andC_0 is initially logic0. Intermediate signals are areG_i and P_i where S_i and C4 are the final outputs. The final carry i.e. C4 does not depend upon the intermediate bits, it depends only on input bits.

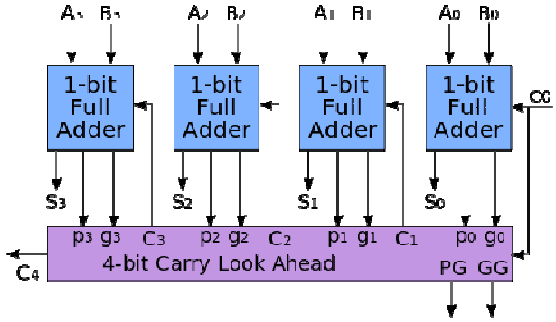

Figure1 : Block diagram of 4-bit CLA

A. Propagation

B. Generation

C. Implementation

Substituting C_1intoC_2, then C_2into C_3, then C_3into C_4yields the expanded equations:

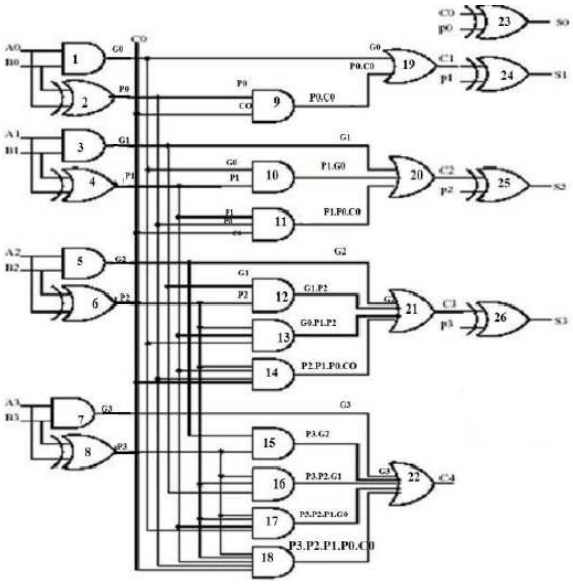

Figure 2: Gate level architecture of 4-bit CLA

III. DESIGN METHODOLOGY

In this section CLA is implemented using Standard CMOS logic, Differential Cascade Voltage Switch (DCVS),Pseudo NMOS logic, Pass Transistor Logic (PTL) ,Domino logic and modified CLA.

A. Standard CMOS logic

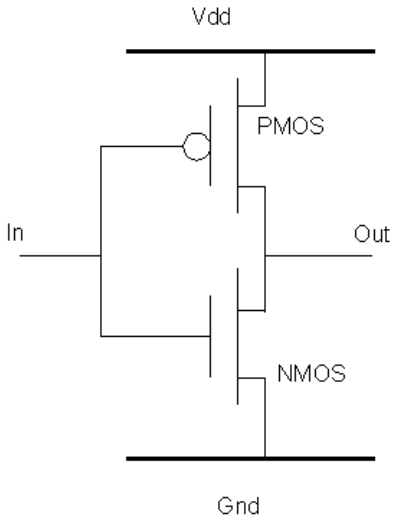

Figure 3: Block diagram of standard CMOS logic

The most widely used logic style is Standard CMOS. The PMOS devices are used in PUN and NMOS devices are used in PDN[4,6]. The advantages of CMOS are 1) outputs are well defined 2) output does not change with time, 3) Clock is not required for refreshing the voltage of nodes 4) Robust structure 5) Low power consumption with no static power dissipation in ideal situation. The drawbacks are 1) The number of gates required for N fan-in gate is 2N and hence occupies large area 2) The propagation delay of a complementary CMOS gate deteriorates rapidly as a function of a fan-in.

B. DCVS logic

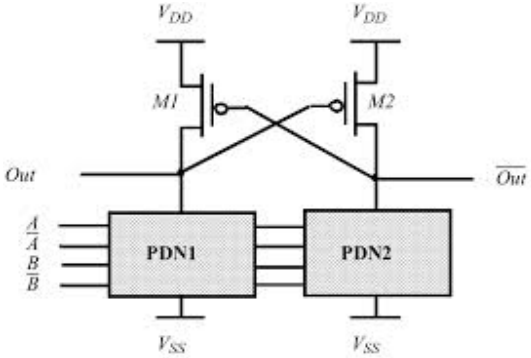

Figure 4: Block diagram of standard DCVS logic

The DCVS logic provides differential outputs [7]. Both the output and its inverted value are simultaneously available. The differential implementation reduces the number of gates required by a factor of two.

The advantages of DCVS are 1) High speed 2) Both the true and the complementary inputs and output are used 3) Ideally zero static power.

The drawbacks of this logic are 1) high dynamic power dissipation 2) More interconnection required as 2 wires are required to represent one signal.

C. Pseudo NMOS logic

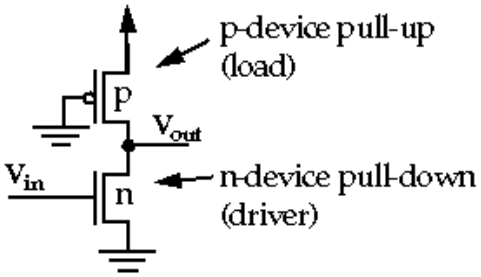

Figure 5: Block diagram of pseudo NMOS logic

Pseudo NMOS logic design is one of the ways to reduce the transistor count [3,4]. Pull up network is grounded, so it is always ON. The main reason is to improve the noise margin and speed. Purpose of PUN is to provide a conditional path between V_{DD} and the output when Pull down network(PDN) is OFF. This logic is also called as ratioed logic. The advantage of Pseudo NMOS logic are1) low area as only N+1 transistors are needed for an N-input gate 2) low input gate-load capacitance.
The drawbacks of pseudo NMOS are 1) static power dissipation.

D. Pass Transistor Logic

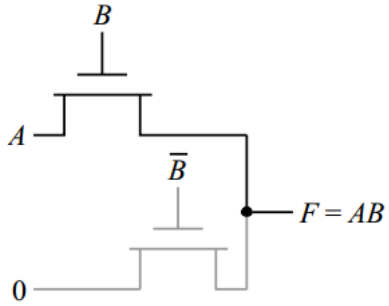

Figure 6: Block diagram of PTL logic

A popular and widely used alternative for complementary CMOS logic is pass transistor logic. It reduces the count of transistors used to make different logic gates by eliminating redundant transistors. In conventional logic families input is applied to gate terminal of transistors but in the case of PTL the input is applied to the source ,drain and gate terminals. Static power dissipation is unaffected.
The above figure shows the implementation of AND function using only NMOS transistors. Its presence is essential to ensure that the gate is static; that is a low impedance path exists. When B is 1 top device turns on and copies the input A to output F. when B is low bottom device turns on and passes a 0.The advantages of this logic are 1) fewer devices to implement the logic functions as compared to CMOS 2) Both gate and source/drain are used as input ports. The drawbacks of PTL are 1) Static power dissipation, 2) Low noise immunity 3) Limited output swing.

E. Domino logic

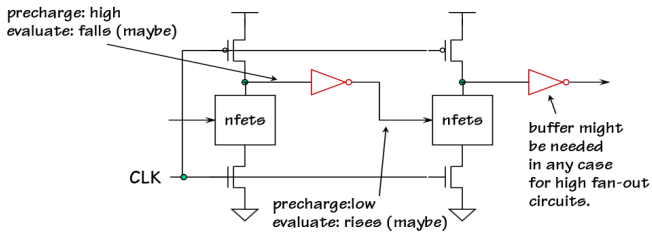

Figure 7: Block diagram of domino logic

Domino logic consists of an n-type dynamic block followed by a static invertor.
When CLK is low, dynamic node is pre-charged high and buffer inverter output is low. N-type in the next logic block will be off. When CLK goes high, dynamic node is conditionally discharged and the buffer output will conditionally go high. Since discharge can only happen once, buffer output can only make one low-to-high transition. The introduction of static inverter has an additional advantage that the fan-out of the gate is driven by a static inverter with a low impedance output, which increases noise immunity. The buffer further more reduces the capacitance of the dynamic output node by separating internal and load capacitances.
Now let us consider chain of domino gates. During pre-charge all the inputs are set to zero. During evaluation, the output of first domino block is either zero or there is a transition from zero to one, affecting the second gate.
Since each dynamic gate has a static inverter, only non-inverting logic can be implemented. Although there are ways to deal with this, this is a major limiting factor. Obtaining pure domino design has become rare.
The advantages of domino logic are 1) The output capacitance is smaller leading to high speed during switching time due to elimination of PMOS transistors 2) Noise sensitive.
Drawbacks of domino logic are, 1) Charge leakage, 2) Charge sharing, 3) CLK is always required, 4) cannot operate at low frequency.

F. Modified CLA

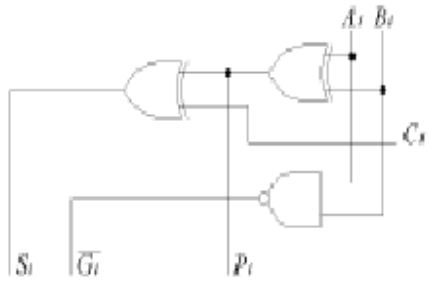

Figure 8: Metamorphosis of partial full adder

The modified Carry-look ahead adder is constructed in the same way as CLA. It contains arithmetic adder circuit and carry-look adder circuit [8]. In the modified CLA, all of the AND gates are replaced with NAND gates except for the AND gate of P bit.
In mathematics, a K^m bit CLA model is defined. Where K is the number of bits consisted in each level of CLA and m is the level of carry look ahead adder circuit used in CLA.

The carry of the next stage is explained as

$$C_{I+1} = \overline{\overline{G_1}.\overline{P_1 C_1}}$$

The carry output of each stage can be listed in the following

$$C_0 = Input\ Carry$$
$$C_1 = \overline{\overline{G_0}.\overline{P_0 C_0}}$$
$$C_2 = \overline{\overline{G_1}.\overline{P_1 G_0}.\overline{P_1 P_0 C_0}}$$
$$C_3 = \overline{\overline{G_2}.\overline{P_2 G_1}.\overline{P_2 P_1 G_0}.\overline{P_2 P_1 P_0 C_0}}$$
$$C_4 = \overline{\overline{G_3 P_3 G_2 P_3 P_2 G_1 P_3 P_2 P_1 G_0 P_3 P_2 P_1 P_0 C_0}}$$

The functions of inverse group generate and the group propagate for 4^m bit can be expressed as,

$$G = \overline{\overline{G_3 P_3 G_2 P_3 P_2 G_1 P_3 P_2 P_1 G_0}}$$
$$P = P_3 P_2 P_1 P_0$$

Therefore c_4 of second level can be produced from G,P and C_0 From first level which is

$$C_4 = \overline{\overline{G P C_0}}$$

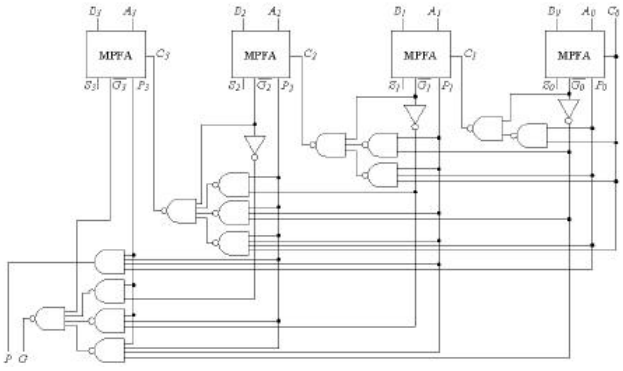

Figure 9: Block diagram of 4-bit MCLA

IV. PERFORMANCE PARAMETERS OF CLA

A. Power dissipation

Power dissipation is a measure of rate at which energy is dissipated or lost from an electrical system. The rate of heat transfer (joules per second) is termed as power dissipation in watts. The DC or average power dissipation is the product of dc supply voltage and the mean current taken from the supply. Power dissipation in CMOS circuits comes from two components.
Static dissipation due to

- sub threshold conduction through OFF transistors
- tunneling current through gate oxide
- leakage through reverse-biased diodes
- contention current in rationed circuits

Dynamic dissipation due to

- charging and discharging of load capacitances

Short circuit current due to

- partially ON state of PMOS and NMOS networks.

Another component in dynamic dissipation is charging and discharging of parasitic capacitances which consume most of the power used in CMOS circuits. This leads to the conclusion that CMOS power dissipation depends on the switching activity by a parameter α, then we can compute the whole power dissipation through the following equation,

$$P = \alpha C_L V_{DD} F_{clk} + (I_{SC} + I_{Leakage}) V_{DD}$$

Where f is the clock frequency of logic operation, CL is the total capacitance charged and discharged every cycle and VDD is the power supply voltage. I_{SC} and $I_{Leakage}$ are the short circuit current and leakage current repectively.

B. Propagation delay

The propagation delay is defined as time required to reach $0.5V_{DD}$ of output from the 0.5 V_{DD} of input. The propagation delays of CLA are measured in order of Nano second.

C. Power Delay Product

Power delay product is the product of average power dissipation and the propagation delay. It is measuredin fJ(10^{-15}).

V. SIMULATION RESULTS AND DISCUSSIONS

All simulation results are obtained from Tanner simulation tool. Comparison ofdifferent logic styles has been done. Further comparison is done with modified CLA also. Power dissipation, Propagation delay of Sum and carry and their powerdelay product are measured. Table1 shows the performance analysis of CLA using different logic styles. Table2 shows the performance analysis of Modified CLA. Figure10 demonstrates the graphical representation of power

consumed by different logic styles.Figure11 shows the propagation delay of sum and carry of CLA using various logic styles. Pseudo has the lowest delay of sum while PTL has the highest delay.Figure12 demonstrates the comparative

Logic Style	No. of transistors	Avg. power consumed (mW)	Propagation Delay (ms)		PDP (fJ)	
			Carry	Sum	Carry	Sum
Standard CMOS CLA	416	32.81	0.14369	0.39220	4.71	12.86
DCVS CLA	452	63.19	1.86181	1.19691	117.64	75.63
Pseudo NMOS CLA	258	199.48	2.02954	0.24964	404.85	49.79
PTL CLA	314	258.92	2.02954	1.34031	525.48	347.03
Domino CLA	380	106.02	1.81455	1.46221	192.37	155.02

Table 1: Simulation Results of CLA Using Different Logic Styles

analysis of CMOS CLA and CMOS MCLA. CMOS MCLA has low power when compared to CMOS CLA. Figure13 shows the comparative analysis of propagation delay of CMOS CLA and CMOS MCLA. CMOS MCLA has time delay of sum lower than that of CMOS CLA.

Figure14 shows the number of transistors used in different logic styles and DCVS has the highest number of transistors and lowest is for CMOS MCLA.

Logic style	No. of transistors	Avg. power consumed (mW)	Propagation Delay (ms)		PDP (fJ)	
			Carry	Sum	Carry	Sum
CMOS MCLA	244	24.51	0.1694	0.10945	4.15	2.68

Table 2: Simulation Results of CMOS MCLA

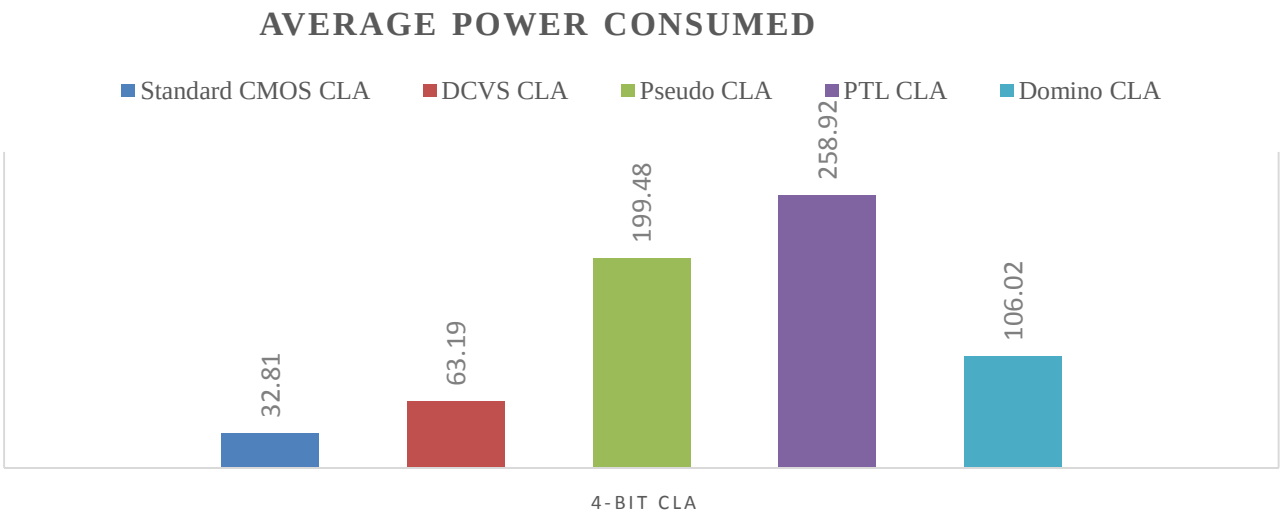

Figure 10: Graphical representation of Average power consumed by CLA when implemented Using Different Logic Styles.

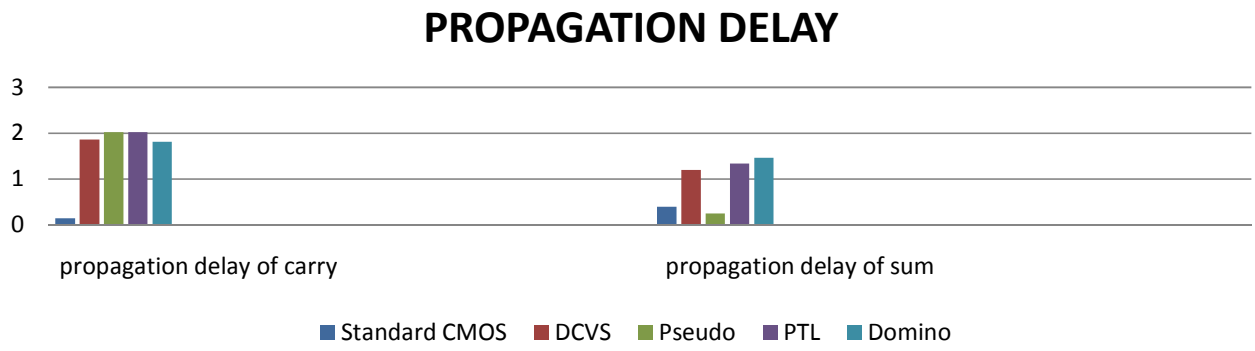

Figure 11: Graphical representation of Propagation delay of sum and carry by CLA when implemented Using Different Logic Styles.

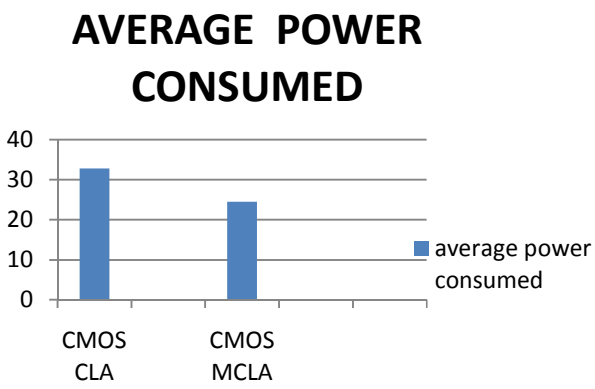

Figure 12: Graphical representation of average power consumed of CMOS CLA and CMOS MCLA.

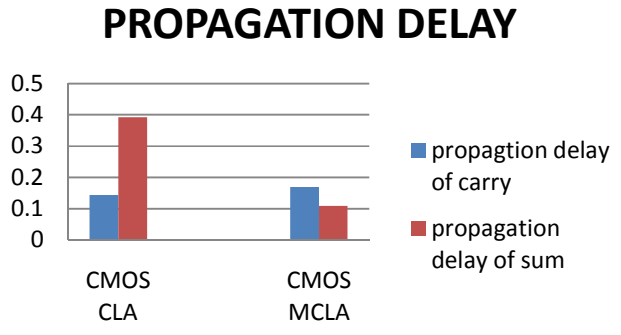

Figure 13: Graphical representation of propagation delay of carry and sum of CMOS CLA and CMOS MCLA.

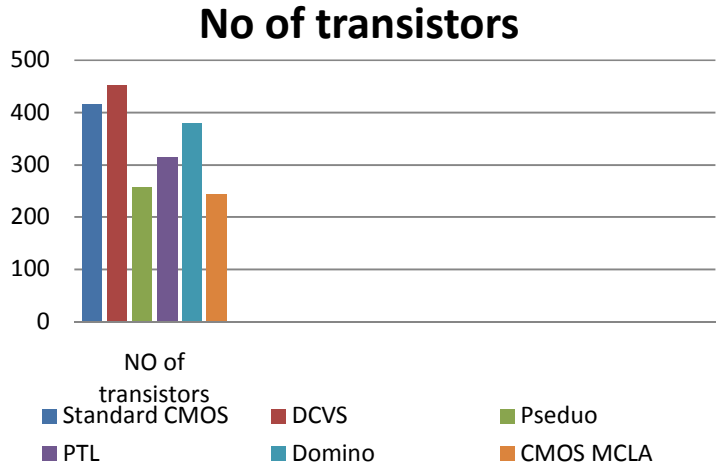

Figure 14: Graphical representation of No of transistors used of different logic styles and CMOS MCLA.

VI. CONCLUSION

A Comparative analysis of CLA using different logic styles shows that standard CMOS has the lowest average power consumed and power delay product. Also the modified CLA uses NAND gate which simplifies and consumes low power than the Carry-Look Ahead Adder Circuit. CMOS MCLA has the lowest power consumption, lowest number of transistors and propagation delay. This circuit may be useful for speeding up other digital logic circuits and for the designers to implement any type of digital VLSI adder circuits.

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