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COMPARATIVE ANALYSIS OF 16:1 MULTIPLEXER AND 1:16 DEMULTIPLEXER USING DIFFERENT LOGIC STYLES

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***Abstract*— Conventional CMOS is compared with transmission gate logic, pass transistor logic and two adiabatic logic styles namely Efficient Charge Recovery Logic (ECRL) and Improved Efficient Charge Recovery Logic (IECRL). A 16:1 multiplexer and 1:16 demultiplexer using different low power technique are designed and results are compared based on their minimum/maximum power consumption and transistor count. The proposed schematics multiplexer and demultiplexer are simulated using MICROWIND2 and DSCH2 software.**

***Index Terms*—Transmission gate logic, Pass transistor logic, Efficient Charge Recovery Logic, low power.**

I. INTRODUCTION

During recent years the main and highly concerned issue in the low power VLSI design is energy/power dissipation. This is due to the increasing demand of portable systems and the need to limit the power consumption in VLSI chips. In conventional CMOS circuits, the basic approaches used for reducing power consumption are by reducing the supply voltages, on decreasing node capacitances and minimize the switching activities with efficient charge recovery logic. The adiabatic logic works on the principle of energy recovery logic and provides a way to reuse the energy stored in load capacitors rather than the conventional way of discharging the load capacitors to the round and wasting this energy. The Power consumption is the major concern in low power VLSI design technology.

II. MOTIVATION

A. Need for low power design

The requirement for low power design has caused a large paradigm shift where energy dissipation has become as essential consideration as area and performance. Several factors have contributed to this trend. The need for low power devices has been increasing very quickly due to the portable devices such as laptops, mobile phones and battery operated devices such as calculator, wrist watches. These products always put a large attention on minimizing power in order to maximize their battery life. Another motive for low power is associated to the high end products. This is due to the packaging and cooling of such high performance, high density and high power chips are prohibitively expensive. Another consideration low power design is related to the environment. The Micro electronics products become tolerable usage in everyday's life, their need on energy will sharply increase. Therefore the reduction in power consumption reduces the heat generated and so reduces the cost required for extra cooling systems in homes and office.

B. Multiplexer

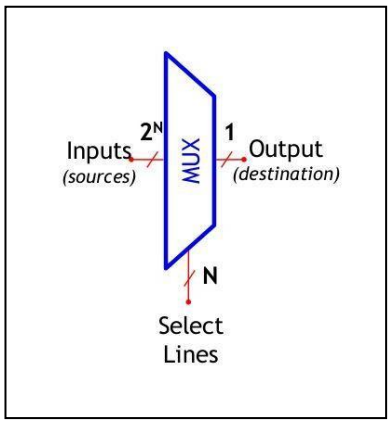


Fig 1: Multiplexer

A multiplexer is a device which selects one of many input signals and forwards the selected input to the output. Block diagram of multiplexer is shown in figure (1). Multiplexers are mainly used connect many sources or devices with single destination or device. A Multiplexer is also known as data selector. Figure (2) shows the function of multiplexer.

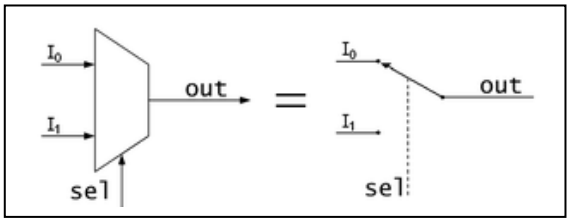


Fig 2: Function of Multiplexer

C. Demultiplexer

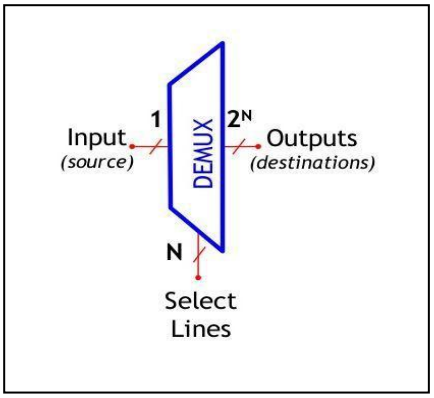


Fig 3: Demultiplexer

A demultiplexer is a device which has single input and many outputs. Demultiplexer is used to connect a single source to multiple destinations. Figure 2 shows the block diagram of demultiplexer. The multiplexer and demultiplexer work together to perform the process of transmission and reception of data in communication system. It performs the reverse operation of multiplexer. Both play an important role in communication systems. Figure (4) shows the function of demultiplexer.

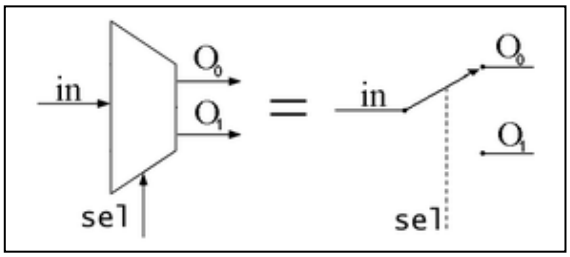


Fig 4: Function of Demultiplexer

LOW POWER TECHNIQUES

Conventional CMOS

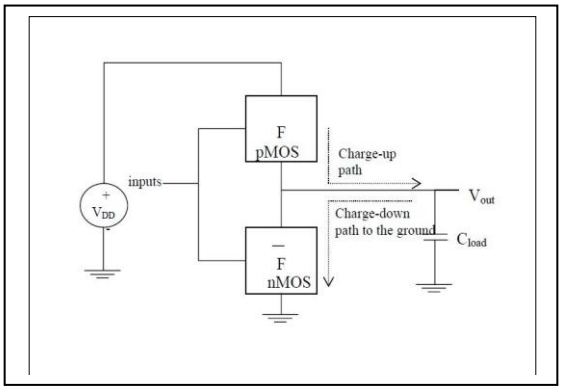


Fig 5: CMOS switching process

Conventional CMOS designs consume a lot of energy during switching process. Two major sources of power dissipation in digital CMOS circuits are dynamic power and static power. Dynamic power is related to the changing events of logic states or circuit switching activities including power dissipation due to capacitance charging and discharging. Figure (1) shows the CMOS switching process.

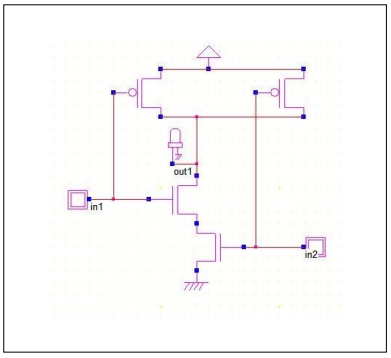
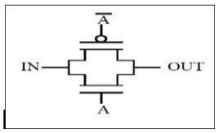


Fig 6: CMOS NAND gate

During device switching, power dissipation primarily occurs in conventional CMOS circuits as shown in figure (1). In CMOS logic design half of the power is dissipated in PMOS network and during the switching events, stored energy is dissipated during discharging process of output load capacitor. CMOS NAND gate is shown in the figure (2) which consists of 2 PMOS and 2NMOS devices.

Transmission gate

The CMOS transmission gate (T-gate) is a useful circuit for both analog and digital applications. It acts as a switch that can operate up to VDD and down to VSS. The CMOS transmission gate utilizes the parallel connection of an NMOS and a PMOS transistor. When the transmission gate is on, it provides a low-resistance connection between its input and output terminals over the entire input voltage range. In transmission gate, the parallel connection of an NMOS and a PMOS transistor acts as a switch. The symbol and truth table of transmission gate is shown in figure (7). A Transmission Gate is a kind of MUX structure.



CONTROL		INPUT	OUTPUT
PMOS	NMOS	IN	OUT
0	1	0	0
		1	1
1	0	0	Z
		1	

Fig 7: Symbol and Truth Table of Transmission Gate

Efficient Charge Recovery Logic (ECRL)

ECRL consists of two cross coupled PMOS transistors and two N-functional blocks for ECRL adiabatic logic block. Both out and out bar are generated. Energy dissipation is reduced to a large extent in ECRL logic by performing the precharge and evaluation phase simultaneously. ECRL dissipates less energy than other adiabatic logics by eliminating the precharge diodes. It consists of only two PMOS switches. It provides full swing at the output. The basic structure of ECRL logic is similar to the Differential Cascode Voltage Switch Logic (DCVSL) with differential signaling. Figure (8) shows the ECRL NAND gate. A major disadvantage of ECRL circuit is that the coupling effects due to the two outputs are connected by the PMOS latch and the two complementary outputs can interfere with each other.

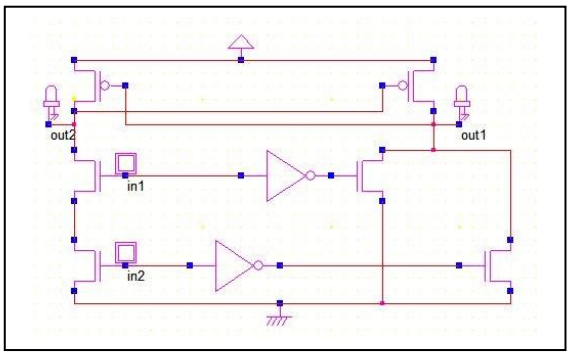


Fig 8: ECRL NAND gate

Improved Efficient Charge Recovery Logic (IECRL)

IECRL consists of a pair of cross coupled PMOS device and two N-functional blocks. In IECRL, delay has been improved by adding a pair of cross coupled NMOS devices in the ECRL design. The basic structure of IECRL is similar to the Modified Differential Cascode Voltage Switch Logic (MDCVSL) with differential signaling. Figure (9) shows the IECRL NAND gate. The IECRL logic is the improved ECRL logic. The performance of IECRL is better than the ECRL logic even though the number of transistors is higher than the ECRL logic. The main advantage of IECRL logic is that it consists of a pair of cross coupled NMOS devices to improve the performance of ECRL logic.

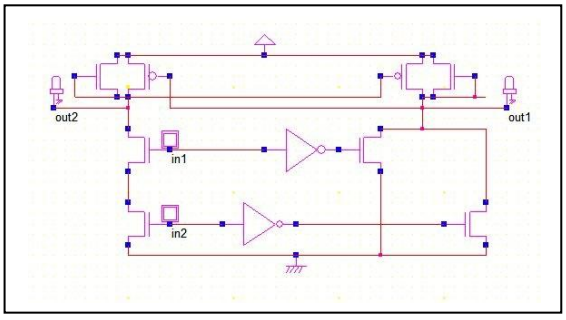


Fig 9: IECRL NAND gate

III. DESIGN AND IMPLEMENTATION

Multiplexer and demultiplexer are used in many applications such as in communication system, many to many switch, ALU design, parallel to serial converter. A 16:1 multiplexer and 1:16 demultiplexer are designed using transmission gate logic, ECRL and IECRL which shows reduce in power dissipation compared to the conventional CMOS logic. The proposed circuit and layout for combinational circuits has been designed in microwind2 version tool and DSCH2 software.

The DSCH2 and Microwind2 are user friendly PC tools for the design and simulation of CMOS integrated circuits. The schematic diagram of all proposed circuits is designed in DSCH software. Using DSCH2, verilog file is generated for schematic diagram of all logic operation. By compiling this verilog file in MICROWIND2, the CMOS layout of the schematic diagram is generated. This layout is simulated in MICROWIND2 to observe the power dissipation of the circuit**.**

16:1 Multiplexer

Figure (10), (11), (12) and (13) shows the 16:1 multiplexer design using Conventional CMOS logic, Transmission gate logic, ECRL and IECRL respectively. The circuits using TGL, ECRL and IECRL are compared with the conventional CMOS based 16:1 multiplexer based on the power dissipation.

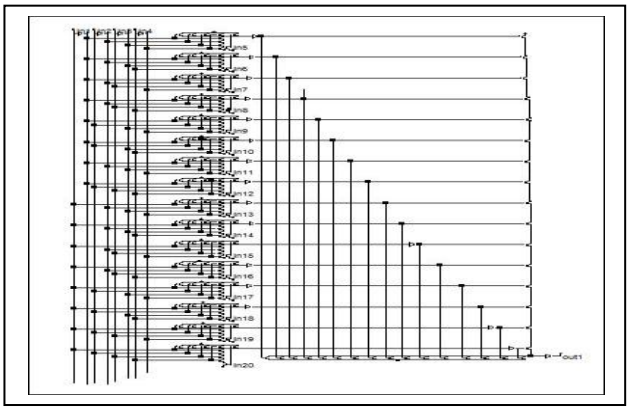


Fig 10: 16:1 Multiplexer using Conventional CMOS logic

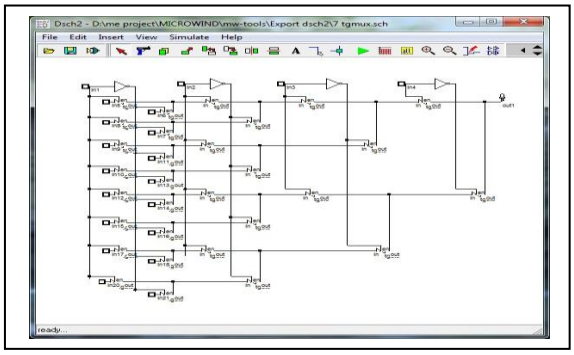


Fig 11: 16:1 Multiplexer using TGL

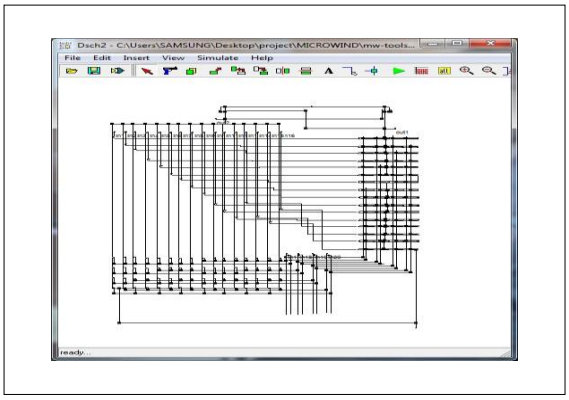


Fig 12: 16:1 Multiplexer using ECRL

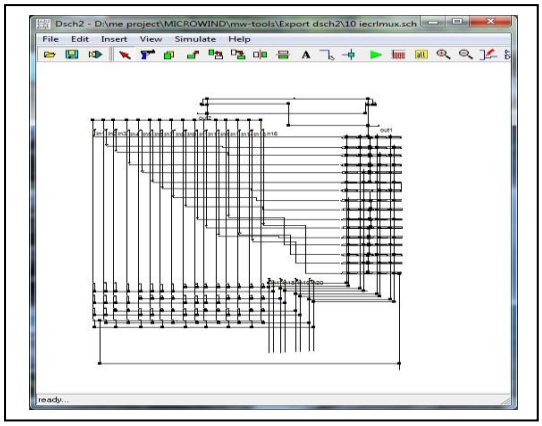


Fig 13: 16:1 Multiplexer using IECRL

1:16 Demultiplexer

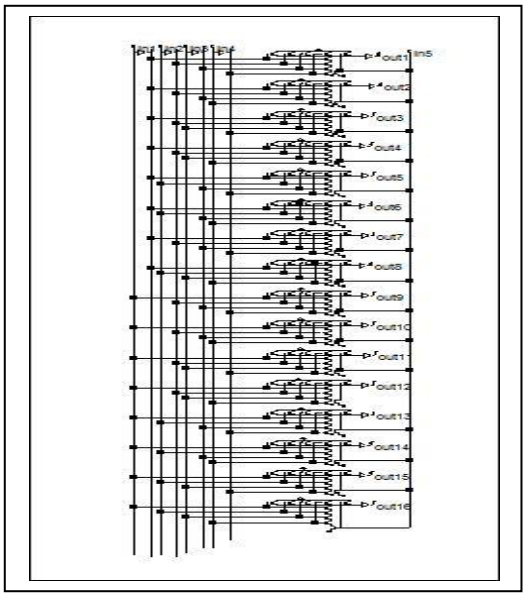


Fig 14: 1:16 Demultiplexer using Conventional CMOS logic

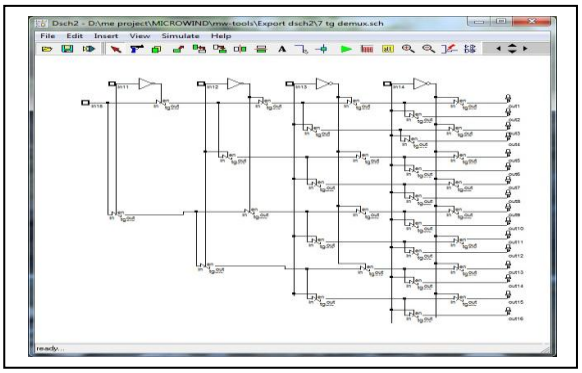


Fig 15: 1:16 Demultiplexer using TGL

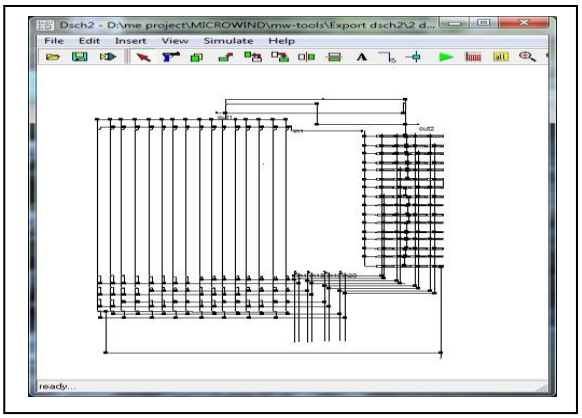


Fig 16: 1:16 Demultiplexer using ECRL

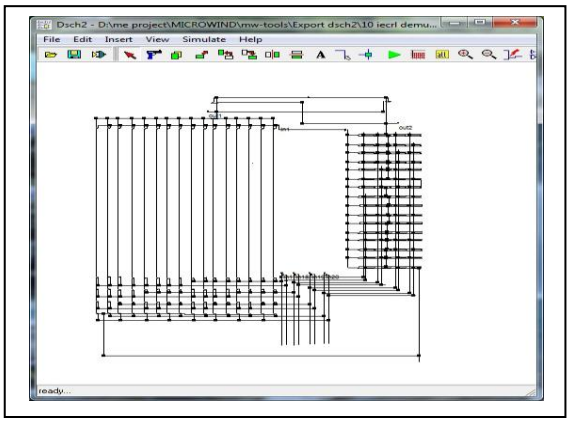


Fig 17: 1:16 Demultiplexer using IECRL

Figure (14), (15), (16) and (17) shows the 1:16 demultiplexer design using conventional CMOS logic, transmission gate logic, ECRL and IECRL respectively. The

circuits using TGL, ECRL and IECRL are compared with the conventional CMOS based 1:16 demultiplexer based on the power dissipation.

IV. COMPARATIVE ANALYSIS

The simulation results are compared based on the power dissipation of the proposed circuits and their transistor count with conventional CMOS logic design.

Technique	**Power dissipation (mW)**	**Number of Transistor**
Conventional CMOS	14.196	192
Transmission Gate logic	14.342	60
ECRL	5.233	162
IECRL	0.239	164

Table 1: Comparison of 16:1 Multiplexer design using different low power techniques

Technique	**Power dissipation (mW)**	**Number of Transistor**
Conventional CMOS	13.105	160
Transmission Gate logic	13.149	60
ECRL	4.946	162
IECRL	0.279	164

Table 1: Comparison of 1:16 Demultiplexer design using different low power techniques

V. CONCLUSION

The proposed combinational circuits primarily focus on lowering the power dissipation. Logics for 16:1 multiplexer and 1:16 demultiplexer are designed and the results indicate that they have lesser power dissipation than conventional CMOS circuits when compares to adiabatic techniques. The power dissipation in conventional CMOS circuits is minimized through adiabatic technique. Adiabatic logic works with the idea of switching activities which reduces the power by offering back the stored energy to the supply. The proposed circuits using ECRL and IECRL are compared with conventional CMOS logic and transmission gate logic for the 16:1 multiplexer and 1:16 demultiplexer. It is observed that the adiabatic technique is good choice for low power application. From the analysis IECRL logic shows significant energy saving compared with conventional CMOS logic, Transmission gate logic and ECRL logic. The future scope of this work is that the proposed 16:1 multiplexers and 1:16 demultiplexers can be cascaded to construct multiplexers and demultiplexers along more number of inputs and output lines.

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