International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)
ISSN: 0976-1353 Volume 8 Issue 1 –APRIL 2014.

Design of Low Power Low Noise Amplifier Using 180nmTechnology

D.Jackuline Moni [#1] and Jenifer.T [*2] , Josephine Agaliya.A [*2]
[#]Professor , ECE, Karunya University, Coimbatore ,India
[*] IV ECE Students ,ECE Karunya University, Coimbatore, India.

Abstract— **CMOS Low Noise Amplifier (LNA) for low power wireless application is presented. Low Noise Amplifier is the most important key component in radio receiver. The inductive source degeneration LNA is designed to achieve the goal of low power, low noise and a high gain. We use 180nm technology in cadence virtuoso tool to design this LNA.**

The designed LNA delivers the power gain of 21.18dB, minimum noise figure of 55mdB and power consumption of 0.19mW.

Index Terms—**CMOS LNA, low power, low noise, Low Noise Amplifier (LNA)**

1.Introduction

A Low Noise Amplifier which is the front end of the radio receiver plays an important role for the signal amplification in communication systems. A radio receiver gives the usable information to the users by converting the radio waves present in an environment. It has LNA, mixer and filter in which LNA plays the major role of amplification. The basic configuration of LNA comprises of RF amplifier in the middle of input matching and the output matching network. The demand of LNA increases due to the development of the modern technologies such as GPS, Bluetooth, cell phones etc

The LNA amplifies the weak signal received by the antenna in the receiving end. Mostly in wireless communication system the LNA is critical to design because it should provide enough gain from the low power signal which is received by the antenna, not only to make signal to noise ratio degradation but also to sustain signals with low power dissipation .A 50Ω resistor is added to the input of the circuit for input matching and for the maximum gain, low noise figure and low power consumption.

This LNA is presented to satisfy the need for high gain with a low power consumption [1].A full band LNA uses a stagger tuning technique and current reusing structure which gives the flat high gain. The disadvantage is the power gain of 9.7dB [2].A stagger tuning technique of two stacked common source stages is described. The disadvantage is the power gain of 10.5 dB [3]. Low power consumption using gm boosting technique is described in this paper, but it has large power dissipation and instability problems [4].The technique tunes the capacitance of the transistor for good linearity. But it of high cost and not used for low power applications [5].It is based on inductive tuning technique for bandwidth extension. But the noise figure is high [6].To reduce the chip size, resistive feedback is used for input matching to transmit the data over a wide spectrum of frequency. The power gain is up to 10.5 dB. [7].An integrated portable LNA for portable GPS receiver is presented for low power consumption but it cannot be used for wide range of frequencies.[8].Using the shunt capacitive feedback and series transformer feedback, the broadband matching condition is achieved with high flat gain, but the power gain is 11 dB[9].CMOS LNA design compromising noise and linearity performance optimization is presented[10].Ultra wide band LNA using current reusing technique and a high pass input matching network is proposed and its noise figure is up to 6dB.

Section 2 deals with the design of LNA to achieve maximum gain and minimum power consumption Section 3 deals with the design of circuit parameters. Section 4 deals with the simulations and discussions. Section 5 deals with conclusions. Section 6 deals with the reference papers.

2. LNA DESIGN

The design of LNA uses the most popular topology, inductive source degeneration as shown in figure.1.The design of LNA includes minimizing the power consumption reducing the noise figure of the amplifier and to provide sufficient gain. The 50 Ω input impedance is stable and it terminates the unknown length of transmission line to deliver signal from antenna to the amplifier. The low power consumption for few portable systems complicates the design process.
The inductive source degeneration topology is the most advantageous for CMOS amplifiers, since it offers the possibility to achieve good narrow band match and a very small noise figure [11].

At series resonance of the input circuit the impedance is proportional to inductor Ls. By choosing Ls the real term can be made equal to 50 ohms. When Ls chosen we use mathematical operation to find NF min and QL. It also provides negative feedback and it stabilizes the gain. The amplifier is single stage cascaded architecture. In this design the single stage LNA uses source degeneration technique for good noise match. A cascode output stage is added to the source degenerated stage which provides improved gain and reverse isolation.M1 and M3 transistors are of same value.

The Rbias should be a large value, so that the noise current is very small. Lg should be of negligible value so that the noise figure gets reduced .It is cascoded to first stage by using an inductor. First stage is designed using a inductive degeneration LNA, where a current reusing technique is used.

3. CIRCUIT DESIGN

Our proposed circuit is based on inductive source degeneration, in the first stage the transistor M2 is set by the supply voltage .The M1 and M2 transistor has the same value. Rbias should be a large value so that the noise current is very small. The M0 transistor is common source configuration and M1 is of common gate configuration. The source inductance Ls provides negative feedback and stabilizes the gain.

The inductive source degeneration LNA is used for an essential noise figure and the maximum gain. The 50 ohm resistor is used at the input for impedance matching. This circuit is advantageous because it is of low power consumption and provides high gain. The inductor is added to the source degeneration LNA by current reusing technique.

The first cascoded stage is connected to the M1 transistor by an inductor. The inductive source degeneration method has an advantage that it has a greater control over the value of real part of impedance by choosing the value of the inductor. The transistor M0 is used to reduce the interaction of the tuned output to the tuned input. The circuit is designed in 180nm technology for a high gain, low noise and low power consumption. The circuit is shown in figure.1

The width and length of the M0 transistor is 50um and 180nm. The width and length of the M1 transistor is 50um and 900nm.And the width and length of the M2 transistor is 50um and 180nm.The value of resistor R0 is 400Ω, R2 is 100uΩ, the value of capacitor C0 is 90pF, C1 is 500aF, the inductor values are L0 is 4nH, L2 is 200aH, L3 is 500aH, L7 is 500nH and L8 is 700nH.

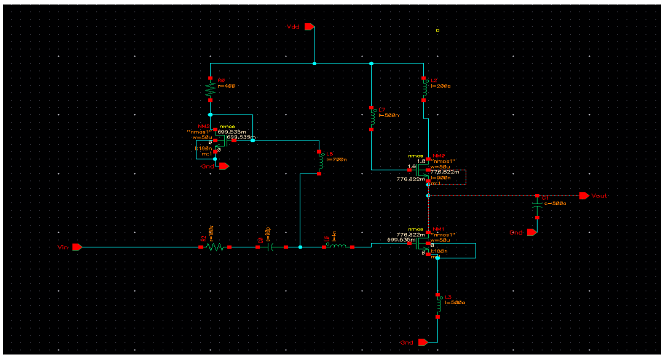

Figure.1 LNA Schematic

4. SIMULATION RESULTS:

Inductive degeneration topology of LNA has good performance on signal to noise ratio in modern communication circuit .The demand of miniature and compact in small area is a feature tread for manufacture. Owing to this necessity the source inductor is of negligibly small value to provide the negative feedback and stabilizes the gain.

The design of LNA is challenge because of its simulation requirements for high gain, low noise figure, good input and output matching and unconditional stability at lowest possible current drawn from the amplifier.LNA is required to extract the incoming signal which is amplified from the noisy environment.

There are certain parameters which are very important in design and verification of Low Noise Amplifier. The parameters are stimulated and presented below.

(a)AC Input Signal:

This signal shows the analysis of power in terms of alternative current the graph is plotted between time in second and voltage in volts. In the input signal given to the amplifier is of 1V and the amplified output signal is shown in figure.2

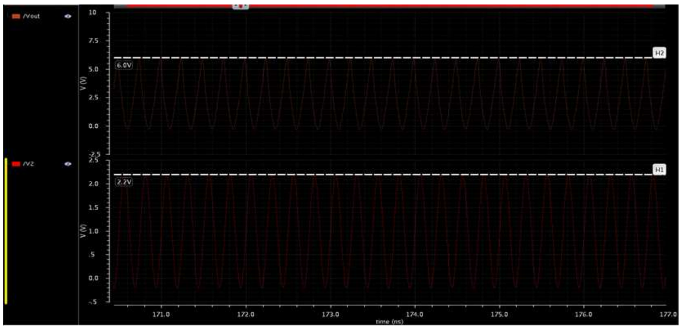

Figure.2 Output Amplification

(b)Gain at frequency 2.4GHz:

The power gain is defined as the ratio between the power available from the network and the power available from the source. This power gain shows the maximum possible power amplification of the amplifier. The gain achieved in this circuit is 21.1dB. The achieved gain is shown below in the figure. 3

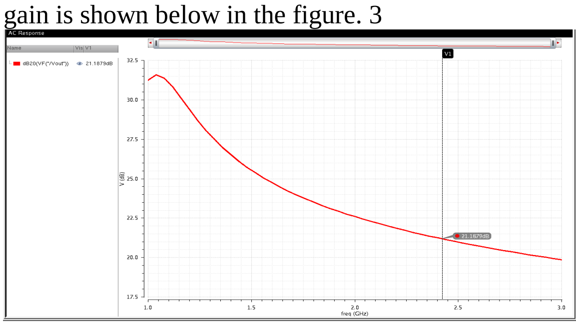

Figure.3 Gain at frequency 2.4GHz

(c) Noise Figure:

The noise performance of the LNA amplifier is represented by its noise factor or noise figure. The overall noise figure is mainly determined by the first amplification stage, provided that it has a sufficient gain. The noise figure is calculated by using this formula

NF=NFmin + matched network factor (1)

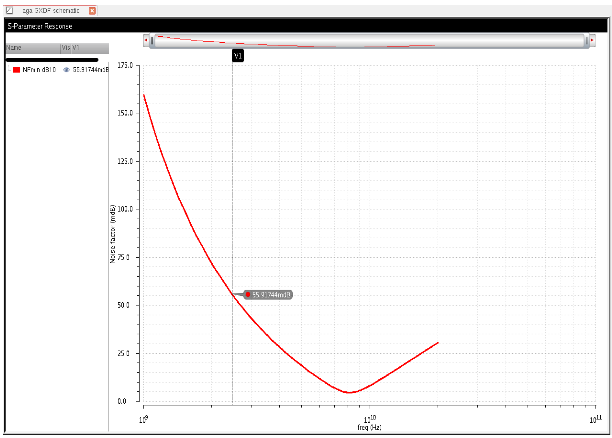

Figure.4 NFmin

The LNA should not send too much noise to the radio receiver. Because it amplifies the weaker signals. Hence designing the LNA with a low noise figure is a crucial process. The minimum noise figure is 55mdB.

The noise figure achieved for this circuit is 4.8dB. The noise figure graph is shown below in the figure.5

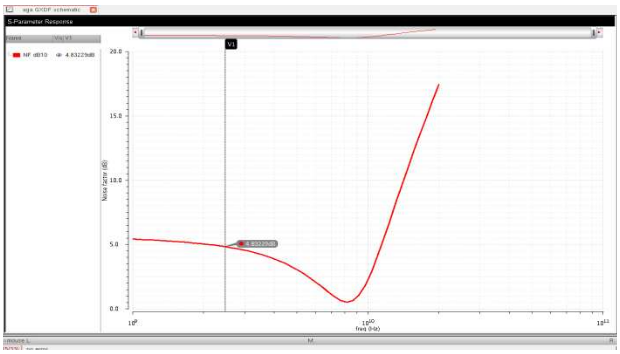

Figure.5 Noise Figure

(d)Power consumption and Supply voltage:

Most of LNA operates on class A mode. The power consumption should be less in order to design budget. The supply voltage for this circuit within its design budget. The supply voltage for this circuit is 1.8V .The power consumption is 0.19mW power calculation of this Low Noise Amplifier is shown in figure.6

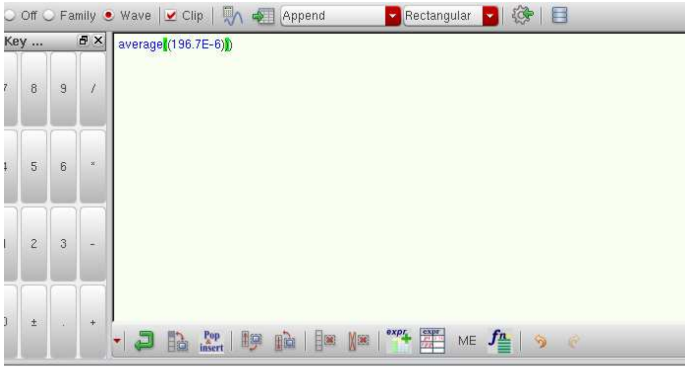

Figure.6 Power Calculation

S-Parameters:

The S–parameters are also called as Scattering parameters which are widely used in microwave and radio frequency techniques. This is used to find the stability analysis for LNA circuits.

(1) S11:

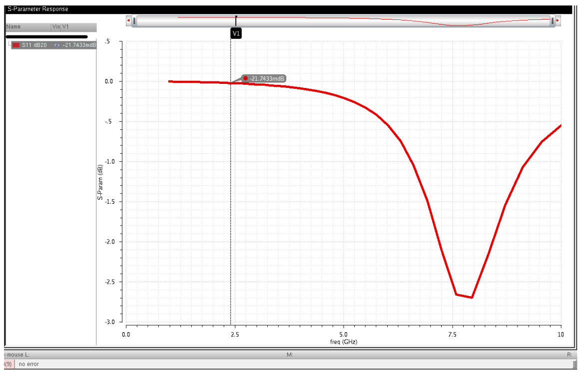

Figure.7 S11 graph

The S11 parameter defines the reflected power back from the input. The S11 value is -21.71dB. The graph of S11 is shown in figure .7

(2) S12:

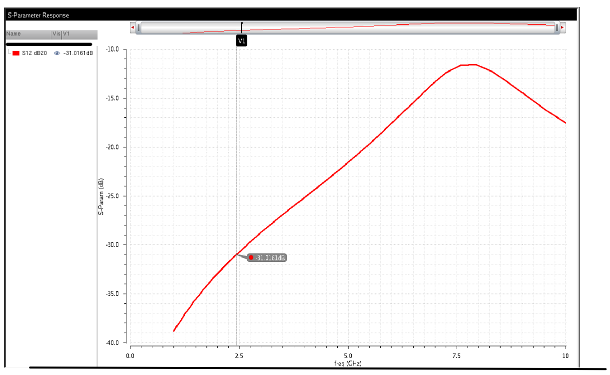

Figure.8 S12 graph

The S12 is the reverse power back from the output to input. The value of S12 is -31.061db.The graph of S12 is shown in figure.8

(3) S21:

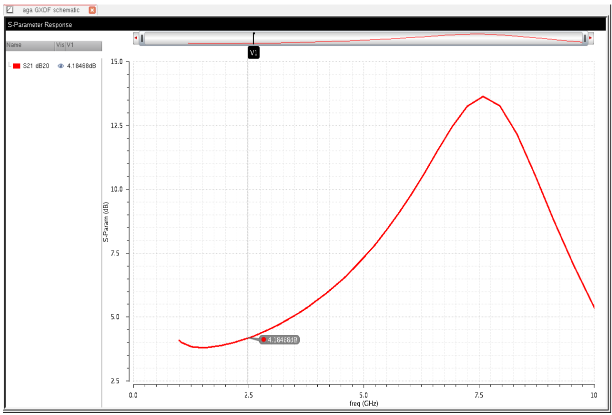

Figure.9 S21 graph

The S21parameter is the forward power from the input to the output.the value of S21 is 4.1dB.the graph of S21 is shown in the graph.9

(4) S22:

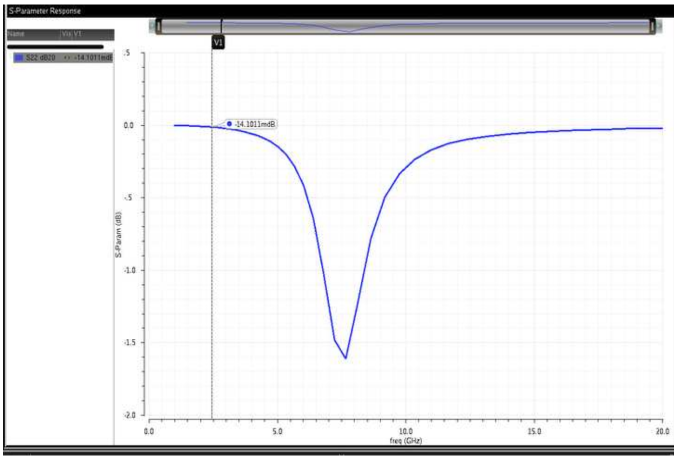

Figure.10 S22 graph

The S22 parameter is the reflected power back from the output.The value of S22 is -14.2dB.The graph of S22 is shown in figure .10

5.CONCLUSION:

Table .1

Parameters	[1]	[2]	[3]	[4]	[5]	This work
Gain(dB)	9.7	10.9	17.5	16.4	>12	21.18
Noise Figure(dB)	5.2-7	3.5	1.9-3.3	2.9-4.6	4.4-5.3	55mdB-4.8dB
Power Consumption (mW)	4.5	7.1	10.6	3.9	4.5	0.19
Power Supply(V)	1.5	1.8	1.8	1.8	1.8	1.8

This table.1 shows the comparison of the values between this work and all the other reference papers.

The LNA is the main part of radio receiver.All design parameters reflects the quality of a Low Noise Amplifier. The LNA is designed to amplify the weak signal to provide the appropriate working condition to the mixer and to attenuate the noise level. This paper highlights the design challenges providing an excellent gain of 21dB and power consumption of 0.19mW. The S-parameters are more applicable due to its ability to express interms of powers suitable for high frequency applications and possibilty of complete transmission.

6.REFERENCES

[1] R M Weng,C Y Liu ,and P C Lin,"A Low power full band low noise amplifier for ultra wide band receivers",IEEE Trans.Microwave Theory and Techniques,Vol 58,no.8pp.2077-83,Jun 2010.

[2] C C Wu,M F Chou,W S Wuen,and K A Wen ,"Low Noise Amplifier for ultra wideband wireless application",In the proceedings of the 2005 IEEE International Symposium on Circuits and systems(ISCAS 2005),Vol.5,pp.5063-6,May 2005.

[3] M Forounzanfar and S Naseh,"High Gain CMOS UWB LNA Employing Thermal Noise Cancellation,In the proceedings of the IEEE International Conference Ultra Wideband(ICUWB 2009),pp.118-22.Sep2009.

[4] A Meanmer,C C Boon,K S Yeo ,and M A Do,"A Wideband Low Power Low Noise Amplifier in CMOS Technology",IEEE Trans.Circuits Syst., Reg. Papers, Vol57,no.4,pp.773-82, Apr.2011 Sungkyang Park and Wonchan Kim,"Design of a 1.8 GHz Low Noise Amplifier for RF front end in a 0.8,"Consumer Electronics,IEEE Transactions on ,Vol 47,No.0098,2001.

[5] S Shekhar,J Waling,and J Walling, and D Allstot,"Bandwidth extension techniques for CMOS amplifiers"IEEE J.Solid-State Circuits,VOL.41,no.11, pp.2424-39,Nov.2006.

[6] M T Hsu and S Y Hsu,"A Low Power Low Noise Amplifier for 1-10GHz Application",In the proceedings of the 2009 IEEE Asia Pacific Microwave Conference(APMC 2009),pp.1132-5,Dec.2009.

[7] W Xia ,and X Zhang ,"A Low Power Low Noise Amplifier for portable GPS Receiver",In the proceedings of the 2009 International Conference an Communications,circuits and systems(ICCCAS 2009),pp.793-6,Jul.2009.

[8] C T Fu,and C N Kuo,"3-11 GHz CMOS UWB LNA Using Dual Feedback for Broadband Maching",IEEE Radio Frequency Integrated Circuits(RFIC) Symposium,pp.54-6,jun.2009

[9] E Roa,J N Soarez,and W Van Noije,"A Methodology for CMOS Low Noise Amplifier",In the proceedings of the 16th Symposium on the integrated circuits and System Design(SBCCI 2003), Sep 2003

[10] Y J Lin ,S S HHsu,J D Jin,and C Y Chan,"A 3.1-10.6 GHz Ultra Wideband CMOS Low Noise Amplifier with Current –Reused Technique",IEEE Microwave and Wireless Componenets Letters.

[11] Neha Rani,"Design of CMOS LNA for Radio Receiver using the Cadence Simulation Tool ",MIT International Journal of ECE,Vol.3,No.2,August 2013,pp.63-68 ISSN No.2230-7664.

First Author

Dr.D.Jackuline Moni working as a Professor in ECE Department, Karunya University. She is in charge of M.Tech (VLSI design) in karunya university.she did her B.Tech in Electronics Engineering at Madras Institute of Technology, Anna University, M.E in (Applied Electronics) from Government College of Technology, Coimbatore, and her Ph.D in (VLSI DESIGN) from Anna University, Chennai. She has over 25 years of teaching experience .She has guided more than 70 UG and PG projects in the area of VLSI design and Embedded systems. She has presented and published more than 60 papers in National and International Journals and conferences. Her areas of interest are CAD VLSI Design, Device modeling, Low Power VLSI Design, analog VLSI and Embedded System Design.

Second Author

Jenifer.T, final year B.Tech ECE student in Karunya University.

Third Author

Josephine Agaliya.A, final year B.Tech ECE student in Karunya University.