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A NOVEL APPROACH TO THE MODULATION OF OQPSK-TYPE TRANSMISSION OVER OFDM TRANSCEIVER

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Abstract **- 4G and other wireless systems are currently hot topics of research and development in the communication field. Orthogonal frequency division multiplexing (OFDM) is the most commonly used modulation scheme for high data rate wireless transmission .In this paper, a OFDM Transceiver has been designed to increase the throughput for future wireless networks .Here the data rate is increased by implementing a 512-point parallelized FFT/IFFT Processor. In the modulation scheme a 16 or 64-OQPSK is implemented. By this work we may obtain a throughput speed between 2Gbps and 4Gbps.**

Index Term **-** OFDM, FFT, IFFT, OQPSK, cyclic prefix.

I. Introduction

The principles of OFDM have been in existence for several epochs. However, in recent years these techniques came into practice in modern communications system. In 4G wireless communication systems, bandwidth is a precious commodity, and service providers are continuously met with the challenge of accommodating more users with in a limited allocated bandwidth. Orthogonal frequency division multiplexing (OFDM) is such a technique which provides an efficient means to handle high speed data streams on a multipath fading environment that causes ISI. The required bit rates are achieved due to OFDM multicarrier transmissions. OFDM systems perform better than a single carrier system particularly in frequency selective channels. It is a multiplexing/multiple access scheme that has many favourable features required for the fourth generation systems. FFT (Fast Fourier Transform)/ (Inverse Fast Fourier Transform) IFFT are the main blocks in OFDM system. They are important in achieving high speed signal processing.FFT helps to transform the signal from time domain to frequency domain where filtering and correlation can be performed with fewer operations.

The OFDM hardware implementation has been done either on ASICs, Vertex based FPGA.ASIC based designs suffer from more time to market factor, high cost and provide less flexibility. Moreover, DSP based designs can only support limited data rates due to lack of parallelism and also they have less number of MAC(multiply and accumulate) units. On the other hand, the modern programmable circuits like an FPGA provides parallel processing system, putting the FPGA computing speed at a significant advantage over DSPs .This paper presents the implementation of OFDM Transceiver on FPGA to improve speed and area simultaneously, by utilizing optimal number of resources in terms of slices, LUTs and multipliers of target FPGA to provide high performance cost effective solution for wireless communication applications.

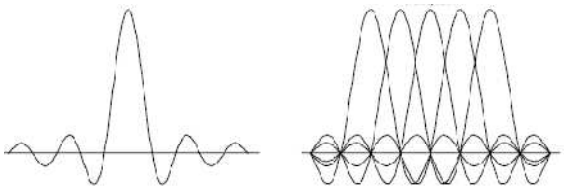


Fig.1: (a) Spectra of an OFDM sub channel and (a) an OFDM signal

II. BASICS OF OFDM

OFDM is a combination technique between modulation and multiplexing. Modulation is a mapping of the information on changes in the carrier phase, frequency or amplitude or their combination. Meanwhile, multiplexing is a method of sharing a bandwidth with other independent data channel. In multiplexing, independent signals from different sources are sharing the channel spectrum. In OFDM, multiplexing is applied to independent signals but these independent signals are a sub-set of the one main signal. In OFDM the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier.

The multicarrier transmission technique uses the discrete Fourier transform. By using a DFT, the whole bandwidth will be split into *N* sub channels.

As a result, a high data stream will be transformed into *N* low rate streams, which are transmitted over different sub-channels. OFDM symbols, which contain several modulation symbols, are formed as linear combinations of mutually orthogonal complex exponentials of finite duration. The splitting of high rate data stream into a number of lower rate streams results in the increase of symbol duration. Mean while a lower rate parallel subcarriers reduces the relative amount of dispersion in time caused by multipath delay spread. Therefore OFDM is an advanced modulation technique which is suitable for high-speed data transmission due to its advantages in dealing with the multipath propagation problem and bandwidth efficiency.

III. OFDM TRANSCEIVER BLOCK DIAGRAM

The block diagram of an OFDM transceiver is shown in Fig. 2

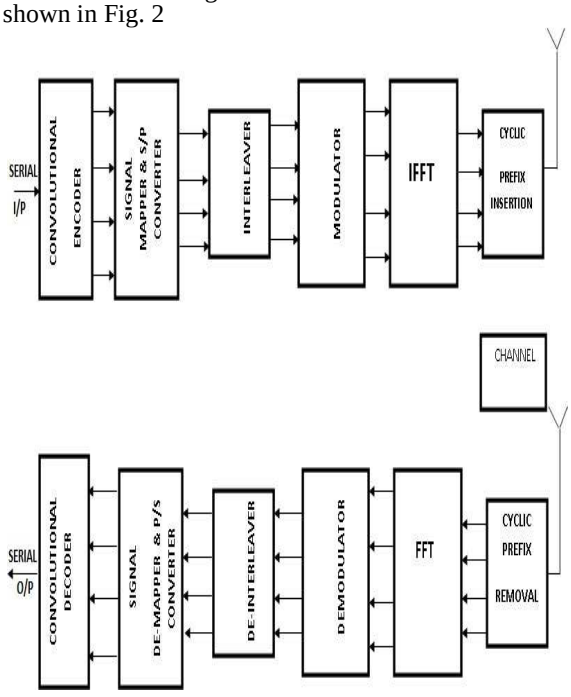


Fig. 2 OFDM Transceiver

A. *OFDM Transmitter*

The main components of OFDM transmitter are shown in Fig.2. The randomizer is used as random bit generator. The first three blocks are used for data coding and interleaving. The coded bits will be mapped by the constellation modulator using Gray codification, this way an + jbn values are obtained in the constellation of the modulator.

The serial to parallel converter converts the data bits from the serial form to the parallel form. The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain.

The Cyclic Prefix (CP) is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame to overcome ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system.

B. *OFDM Receiver*

The main blocks of OFDM receiver are observed in Fig.2. The received signal goes through the cyclic prefix removal and a serial-to-parallel converter. After that, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain.

The output of the FFT is formed from the first M samples of the output. The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the used hardware. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT .

IV. FAST FOURIER TRANSFORM

Discrete Fourier transform (DFT) is a very important technique in modern digital signal processing (DSP) and telecommunications, especially for applications in orthogonal frequency demodulation multiplexing (OFDM) systems. Such as IEEE 802.11a/g [1], Worldwide Interoperability for Microwave Access (WIMAX) [2], Long Term Evolution (LTE) [3], and Digital Video Broadcasting—Terrestrial (DVB-T) [4]. However, DFT is computational intensive and has a time complexity of *O*(*N*2). The fast Fourier transform (FFT) was proposed by Cooley and Turkey to efficiently reduce the time complexity to *O*(*N*log 2*N*), where *N* denotes the FFT size.

A. *FFT and IFFT*

The discrete Fourier transform (DFT) *Xk* of an *N*-point discrete-time signal *xn* is defined by:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \quad 0 \le k \le N-1, \qquad (1)$$

where the twiddle factor , denotes the *N*-point primitive root of unity. However, a straightforward implementation of this algorithm is obviously impractical due to the huge hardware required.

Therefore, the fast Fourier transform (FFT) was developed to efficiently speed up its computation time and significantly reduce the hardware cost. Generally, FFT analyzes an input signal sequence by using a Decimation-in-frequency (DIF) or decimation-in-time (DIT) decomposition to construct an efficiently computational signal-flow graph (SFG). Here, our work employs a DIF decomposition because it matches the manipulation manner of single-path delay pipeline facility. An example of radix-2 DIF FFT SFG for $N = 16$ is depicted in Fig. 3

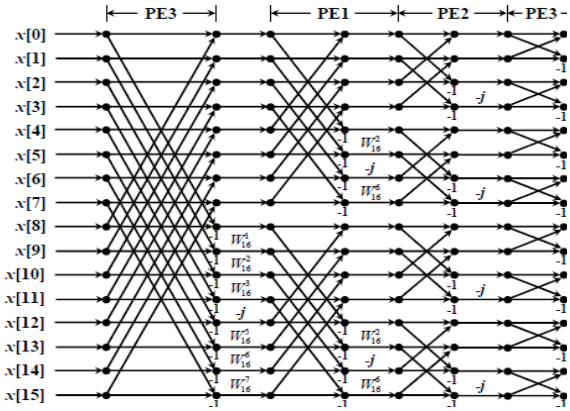


Fig.3 Radix-2 DIF FFT signal-flow graph of length 16

The radix-2 DIF FFT described above appears regularity in SFG and has less complex multipliers required. Thus, it is suited for hardware implementation, because some complex multiplications can be simplified to reduce the chip area.

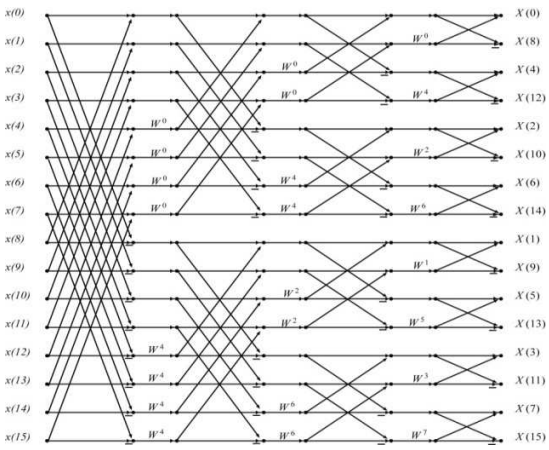


Fig. 4 Radix-2 DIT FFT signal-flow graph of length 16

The inverse discrete Fourier transform (IDFT) of length *N*
is given by:

$$x_n - \frac{1}{N}\sum_{k=0}^{N-1} X_k W_N^{-nk}, \qquad 0 \le n \le N-1.$$

To reuse the same hardware core for reducing the chip area can be rewrite as:

$$x_n = \frac{1}{N}\left(\sum_{k=0}^{N-1} X_k^* W_N^{nk}\right)^*, \qquad 0 \le n \le N-1,$$

Where the star symbol * denotes a conjugate. This new form can be viewed as a general DFT. In other words, DFT and IDFT can reuse the same hardware core, while IDFT requires some extra computations. These extra computations include conjugating the input data *Xk* and the outcomes of DFT, as well as dividing the previous output by *N*. Obviously, this new reuse version of DFT/IDFT algorithm will also simplify the design effort of an DFT/ IDFT processor and thus reduce the chip area, if both the DFT and IDFT processors are activated alternatively, and not simultaneously.

V. MODULATION METHOD

The modulation scheme in an OFDM system can be selected based on the requirement of power or spectrum efficiency. The type of modulation can be specified by the complex number dn=an+jbn. The symbols an and bn can be selected to (1, 3) for 16-OQPSK and 1 for QPSK. Consider a data sequence (d0, d1, d2, dN-1), where each dn is a complex number dn=an+jbn. (an, bn=1 for QPSK, an, bn=1, 3 for 16-OQPSK).

A. Offset Quadrature phase shift keying

OQPSK (offset QPSK) is a special version of QPSK in which the transmitted signal has no amplitude modulation. This disadvantage of a amplitude modulation are a result of 180° shifting in the phase.

In OQPSK the incoming signal is divided in the modulator into two portions I and Q which are then transmitted shifted by a half symbol duration.

Offset Quadrature phase-shift keying (OQPSK) is a variant of phase-shift keying modulation using 4 different values of the phase to transmit. Taking four values of the phase (two bits) at a time to construct a QPSK symbol can allow the phase of the signal to jump by as much as 180° at a time. This produces large amplitude fluctuations in the signal; an undesirable quality in communication systems. By offsetting the timing of the odd and even bits by one bit-period, or half a symbol-period, the in-phase and Quadrature components will never change at the same time. In the constellation diagram shown on the left, it can be seen that this will limit the phase-shift to no more than 90° at a time. This yields much

lower amplitude fluctuations than non-offset QPSK and is often preferred in practice.

Offset QPSK signalling can also be represented by

$$s(t) = \frac{1}{\sqrt{2}} d_I(t) \cos(2\pi f_0 t + \frac{\pi}{4}) + \frac{1}{\sqrt{2}} d_Q(t) \sin(2\pi f_0 t + \frac{\pi}{4})$$

The only difference between QPSK and OQPSK is in the alignment of the two baseband waveforms. Offset between I and Q means that transition is potentially possible every Tb sec.

- In Offset QPSK signalling, sometimes called staggering QPSK, there is same data stream partitioning and orthogonal transmission.
- QPSK (after pulse shaping or filtering) do not have constant amplitude, especially for the transition with a phase shift equal to π.
- Hence, after non-linear power Amp, distortion creates more spectral side lobes (spectral re-generation).
- In offset QPSK, I and Q channels are offset in time by half of a symbol period.
- Phase transitions happen at every half of a symbol period (instead of every symbol period as in QPSK), but each transition is limited to +/-90 degree.
- Results: relatively more constant envelope after pulse shaping.
- Used in the reverse link for IS 95 (CDMA) standards.

B. Constellation Diagram

A constellation diagram is the representation of a digital modulation scheme on the complex plane. The diagram is formed by choosing a set of complex numbers to represent modulation symbols. These points are usually ordered by the gray code sequence. Gray codes are binary sequences where two successive values differ in only one digit. The use of gray codes helps reduce the bit errors. The real and imaginary axes are often called the in-phase and the Quadrature. These points are usually arranged in a rectangular grid in OQPSK, though other arrangements are possible.

The number of points in the grid is usually a power of two because in digital communications the data is binary. Upon reception of the signal, the demodulator examines the received symbol and chooses the closest constellation point based on Euclidean distance.

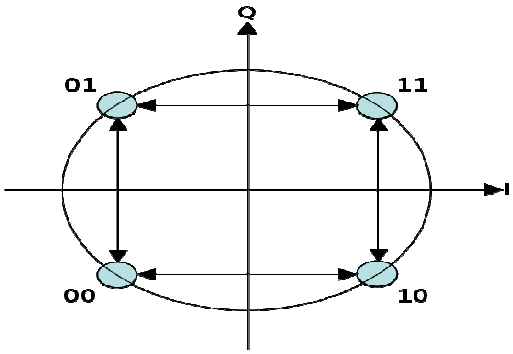


Fig.5: OQPSK Constellation Diagram

It is possible to transmit more bits per symbols by using a higher-order constellation OQPSK, but this is more susceptible to noise because the points are closer together, resulting in a higher bit error rate (BER).

VI. CYCLIC PREFIX

The Cyclic Prefix is a periodic extension of the last part of an OFDM symbol that is added to the front of the symbol in the transmitter, and is removed at the receiver before demodulation. Mathematically, the Cyclic Prefix converts the linear convolution with the channel impulse response into a cyclic convolution. This results in a diagonalised channel, which is free of ISI and ICI interference. The Cyclic Prefix has two important benefits:

1. The Cyclic Prefix acts as a guard space between successive OFDM symbols and therefore prevents Inter-symbol Interference (ISI), as long as the length of the CP is longer than the impulse response of the channel.

2. The Cyclic Prefix ensures orthogonality between the sub-carriers by keeping the OFDM symbol periodic over the extended symbol duration, and therefore avoiding Inter-carrier Interference (ICI).

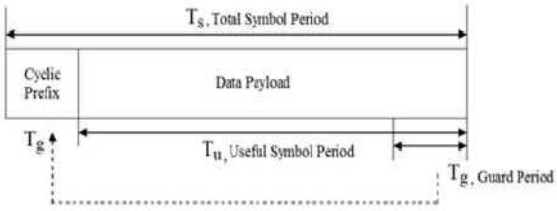


Fig.6**:** Cycle prefix

VII. SIMULATION AND RESULTS

Figure (7) shows the simulated waveform of 512 point FFT processor

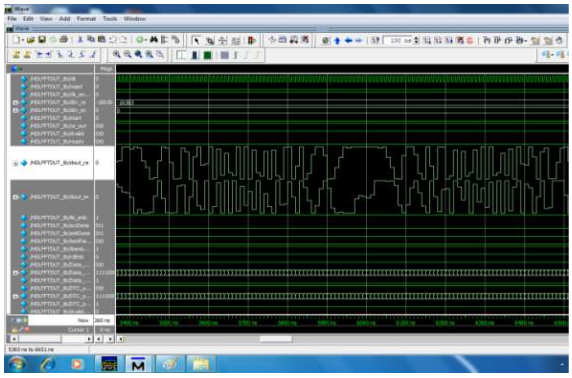


Fig.7: Output waveform of 512 point FFT processor

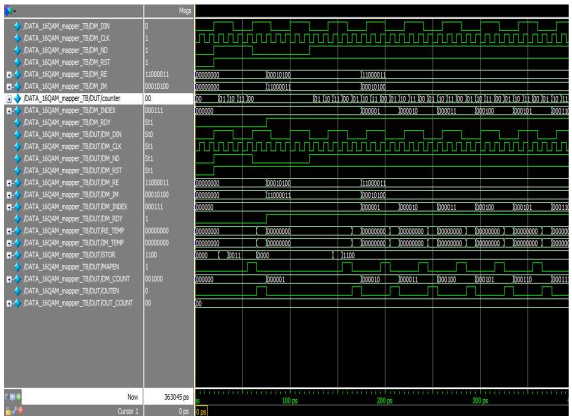


Fig.8: signal mapper

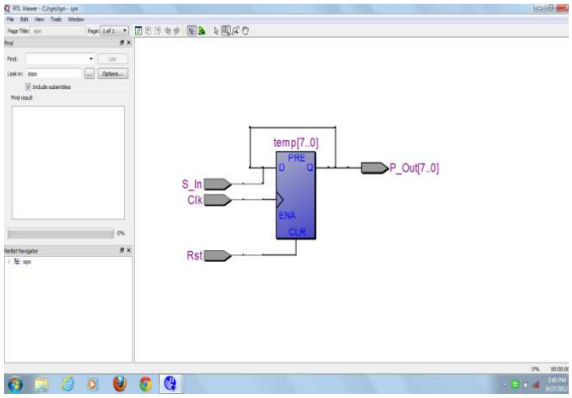


Fig.9: SIPO

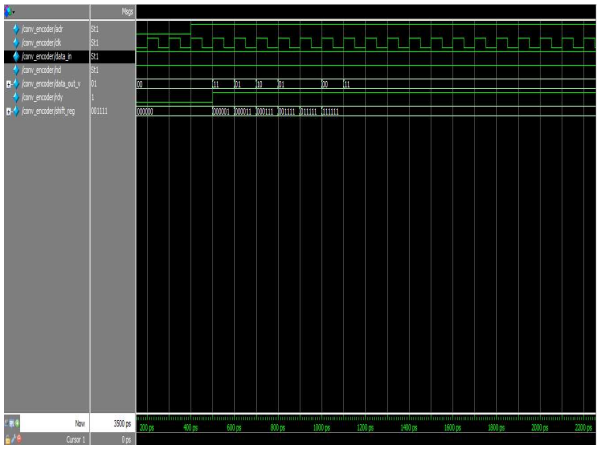


Fig.10: wave Encoder

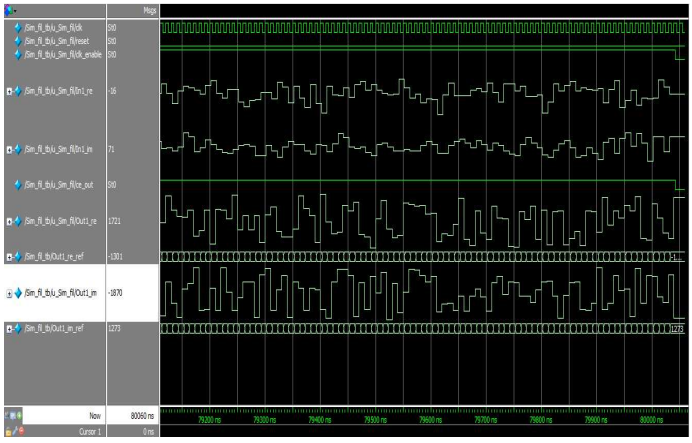
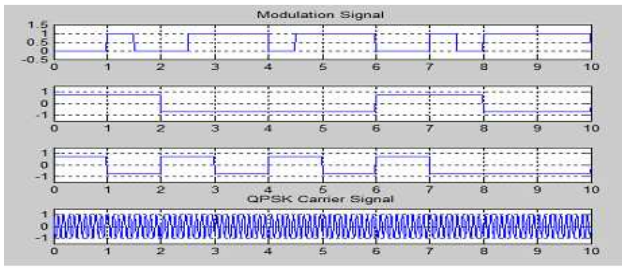


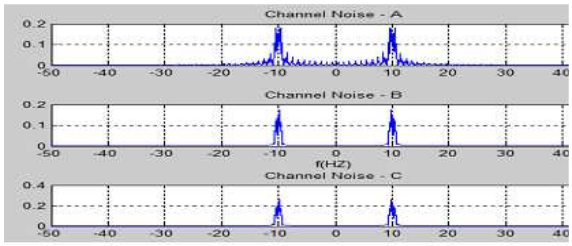
Fig.11 Final output waveform of OQPSK (Modelsim)

QPSK OUTPUT

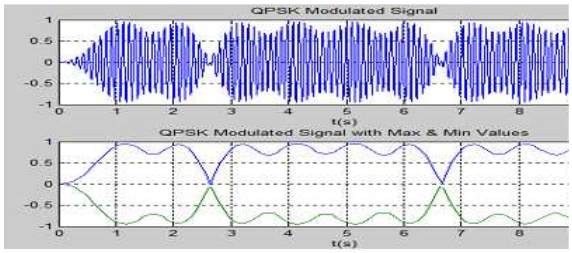
MODULATION



CHANNEL NOISE

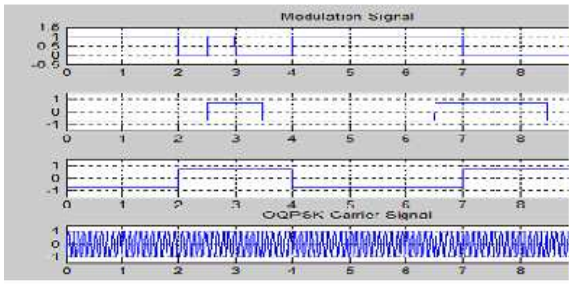


FINAL OUTPUT OF QPSK

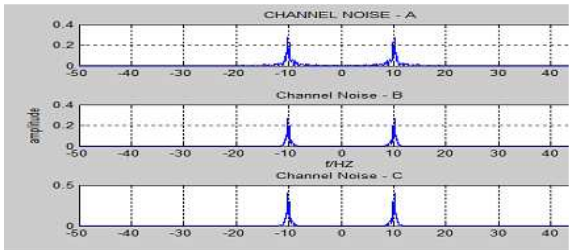


OQPSK

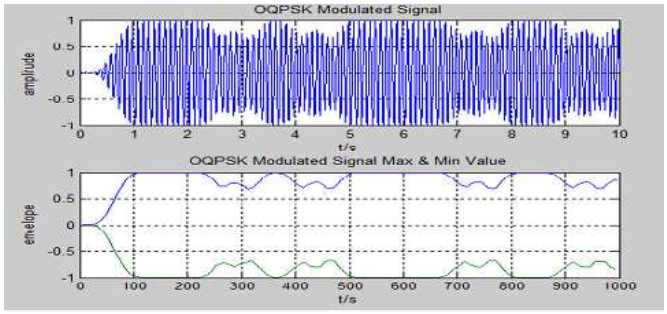
MODULATION



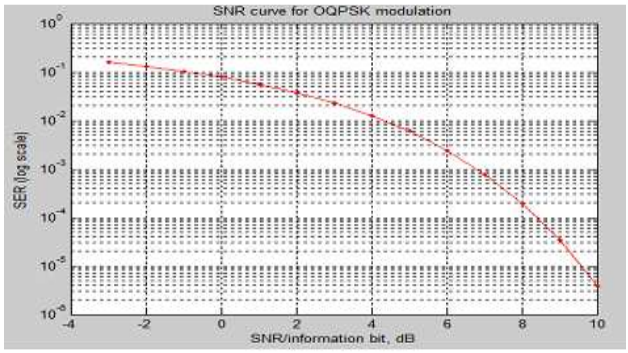
CHANNEL NOISE



FINAL OUTPUT OF OQPSK



SIGNAL TO NOISE RATIO OUTPUT



BIT ERROR RATE OUTPUT

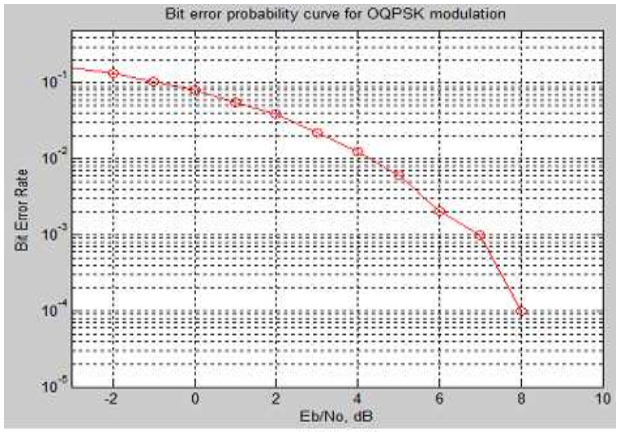


Fig .12: Output waveform of OQPSK (Matlab)

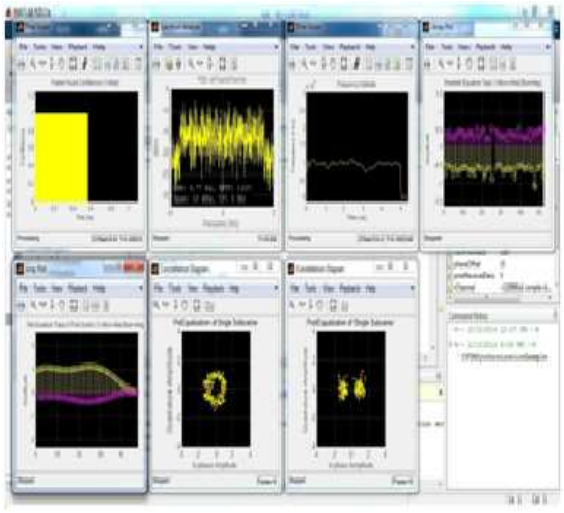


Fig.13 Final output waveform of OQPSK with OFDM system(Matlab)

VIII. CONCLUSION

In this work, we developed a OFDM transceivers based on the proposed architecture which achieves above 2Gbps. Each models of a transmitter and receiver are implemented and simulated. In the following, we present the performance improvement of our pipelined architecture, in terms of the resource utilization. The proposed design has been synthesized and implemented on ALTERA DE1 device board. VHDL code has been generated and simulated using Modelsim.The results show that the design has been simulated up to 227.355 MHz and it achieves higher speed and lower area by using Radix-2 parallelized 512 point FFT/IFFT algorithm. Each FFT stage i.e. radix 2 FFT stage include one radix 2 butterfly computing unit, memory blocks to cache the streaming data, ROM to store FFT twiddle factors, control logic. The memory size of each stage equals the stage number. It is used to reduce the ISI Value. This increases its speed and area factor is also taken care of. The occupied area of an FPGA is proportional to number of used multipliers. The proposed design has shown improvement in area factor also in terms of no. of slices and no. of multipliers. Moreover the proposed design has been implemented on multipliers based lower end FPGAs in order to provide cost effective solution for wireless communication applications.

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