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DESIGN AND SIMULATION OF LOW LEAKAGE HIGH SPEED DOMINO CIRCUIT USING CURRENT MIRROR

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Abstract—**Domino logic is widely used in many applications with high performance and less area overhead. As the technology is scaled down, the supply voltage is reduced for low power and the threshold voltage is also reduced to achieve high performance. Since lowering the threshold voltage leads to an exponential increase of sub-threshold leakage current. Reducing power dissipation has become an important objective in the design of digital circuits. The proposed technique uses an analog current mirror circuit and it is based on comparison of mirrored current of the pull-up network with its worst case leakage current. This technique reduces the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement high-speed and robust circuits. Thus the delay and power consumption are reduced in the wide fan-in domino circuit. The leakage current is also reduced by exploiting footer transistor in the diode configuration. Domino gate that uses an analog current mirror to replicate the leakage current of a dynamic gate pull-down stack and it tracks the process, voltage and temperature using the stacking effect. It improves the performance of the current mirror circuit which will reduce the leakage current.**

***Keywords*— OR gate, domino logic, current mirror, Leakage current**

I. INTRODUCTION

Dynamic logic such as domino logic is widely used in many applications to achieve high performance, which cannot be achieved with static logic styles. However, the main drawback of dynamic logic families is that they are more sensitive to noise than static logic families. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the sub threshold leakage current, reduction of leakage current and improving noise immunity are of major concern in robust and high-performance designs in recent technology generations. However, in wide fan-in dynamic gates, especially for wide fan-in OR gates, robustness and performance significantly degrade with increasing leakage current.

Wide fan-in domino is used for variety of applications like memories and comparators. Domino logic circuit is also a kind of dynamic logic circuit which is used for the high speed and high performance application. Also the domino logic circuit plays a vital role where fan in are high in any circuit. Domino circuits are widely used in high performance microprocessors, register files, ALU, DSP circuits and priority encoders in content addressable memories, such as high fan-in multiplexer or comparator circuits. Thus domino logic circuit techniques are extensively applied in high performance microprocessors due to superior speed and area characteristics.

A. Static Logic Circuits

Static Logic circuits can maintain their output logic levels for indefinite period as long as the inputs are unaffected as shown in Figure 1. Although Static CMOS logic is widely used for its high noise margins, good performance and low power consumption with no static power dissipation, still these circuits are limited at running extremely high clock speeds and suffers from glitches [4]. Number of transistors requires to implement an *N* fan-in gate is almost equal to *2N*; therefore it will consume large silicon area. An alternate logic style is the dynamic CMOS Logic.

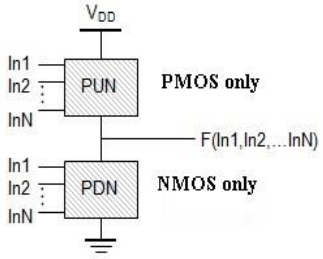

Figure 1. CMOS Static Logic

B. Dynamic Logic Circuits

Dynamic Logic utilizes simple sequential circuits with memory functions. The operation depends on temporary storage of charge in parasitic node capacitances. Dynamic circuits have achieved widespread use because they require less silicon area and have superior performance over conventional static logic circuits. As shown in Figure 2, Dynamic logic uses a sequence of pre charge and evaluation phases governed by the clock to realize complex logic functions [4]- [6].

Pre Charge Phase

When clock signal *(Φ)* = 0, the output node *Out* is pre-charged to *VDD* by the PMOS transistor M_p and the evaluate NMOS transistor M_e remains off, so that the pull-down path is disabled

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Evaluation Phase

In the PDN when clock signal *(Φ)* = 1, the pre-charge transistor M_p is OFF, and the evaluation transistor M_e is turned ON. The output is conditionally set down based on the input values and the pull-down topology.

But the main disadvantage of Dynamic Logic Circuits is that they cannot be cascaded. To overcome this problem Domino Logic came into existence.

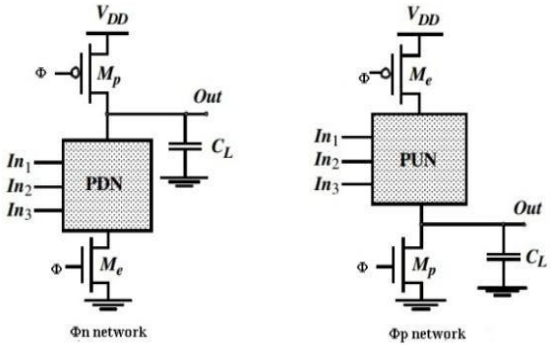

Figure 2. CMOS Dynamic Logic

C. Domino Logic

The name domino comes from the behaviour of a chain of the logic gates. It is a non–inverting structure as shown in Figure 3. It runs 1.5-2 times faster than static logic circuits. It is simply a logic which permits high-speed operation and enables the implementation of complex functions which otherwise is not achieved by Static and Dynamic circuits [4]-[6]. Domino logic offers a simple technique to eliminate the need of complex clocking scheme by utilizing a single phase clock and have no static power consumption as it is removed by clock input in the first stage. These logic circuits are glitch free, have fast switching threshold and possibility to cascade. Domino circuits employ a dual-phase dynamic logic style with each clock cycle divided into a pre charge and an evaluation phase.

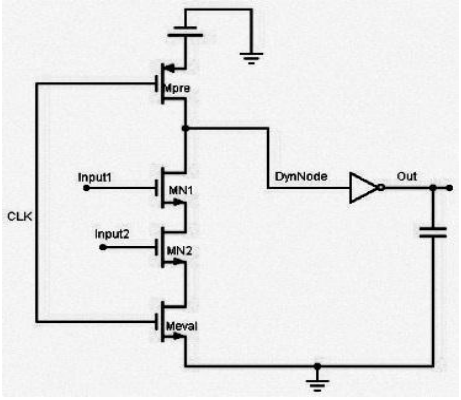

Figure 3. CMOS Domino Logic

II. LITERATURE REVIEW

The most popular dynamic logic is the conventional standard domino circuit as shown in Figure 4. In this design, a PMOS keeper transistor is employed to prevent any undesired discharging at the dynamic node [12] due to the leakage currents and charge sharing of the Pull-Down Network (PDN) during the evaluation phase, hence improving the robustness. The keeper ratio *K* is defined as

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{Keeper}-\text{transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{evaluation}-\text{network}}} \qquad (1)$$

Where *W* and *L* denote the transistor size, and μ_n and μ_p are the electron and hole mobilities, respectively. However, the traditional keeper approach is less effective in new generations of CMOS technology. Although keeper upsizing improves noise immunity, it increases current contention between the keeper transistor and the evaluation network. Thus, it increases power consumption and evaluation delay of standard domino circuits. These problems are more critical in wide fan-in dynamic gates due to the large number of leaky NMOS transistors connected to the dynamic node. Hence, there is a trade off between robustness and performance, and the number of pull-down legs is limited.

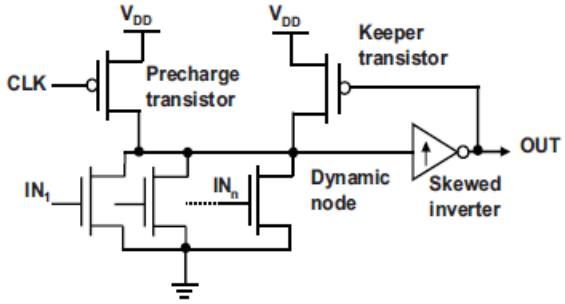

Figure 4. Conventional Standard Domino Circuit

Several circuit techniques are proposed [3] to address these issues. These circuit techniques can be divided into two categories.

1. Changing controlling circuit of the gate voltage of the keeper transistor

2. Changing the circuit topology of the footer transistor

In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as Conditional-Keeper Domino (CKD) [7], High Speed Domino (HSD) [8], Leakage Current Replica (LCR) keeper domino [9], and Controlled Keeper by Current-Comparison Domino (CKCCD) [10]. On the other hand, in the second category, designs including the proposed designs change the circuit topology of the footer transistor or reengineer the evaluation network such as Diode Footed Domino (DFD) [13] and Diode-Partitioned Domino (DPD) [11].

A. Conditional Keeper Domino Logic

Conditional Keeper employs two keepers, small keeper and large keeper. In this technique, the keeper device (PK) in conventional domino is divided into two smaller ones,PK1 and PK2. The keeper sizes are chosen such that PK=PK1+PK2. Such sizing insures the same level of leakage tolerance as the conventional gate but yet improving the speed.

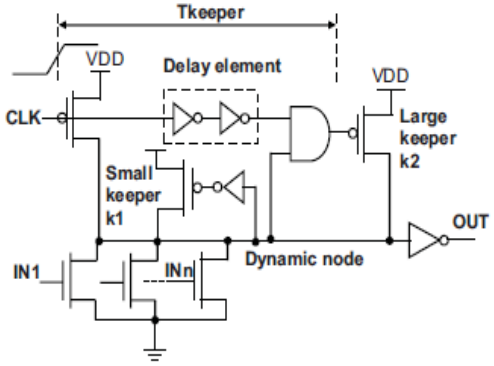

Figure 5. Conditional Keeper Domino

B. High Speed Domino Logic

The circuit of the HS Domino logic is shown in Figure3.8. In HS domino the keeper transistor is driven by a combination of the output node and a delayed clock.

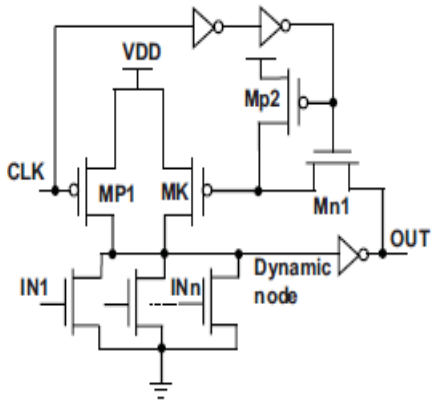

Figure 6. High Speed Domino logic

The circuit works as follows: At the start of the evaluation phase, when clock is high, MP3 turns on and then the keeper transistor MP2 turns OFF. In this way, the contention between evaluation network and keeper transistor is reduced by turning off the keeper transistor at the beginning of evaluation mode. After the delay equals the delay of two inverters, transistor MP3 turns off. At this moment, if the dynamic node has been discharged to ground, i.e. if any input goes high, the nMOS transistor MN1 remains OFF. Thus the voltage at the gate of the keeper goes to VDD-Vth and not VDD causing higher leakage current though the keeper transistor. On the other hand, if the dynamic node remains high during the evaluation phase (all inputs at 0, standby mode), MN1 turns on and pulls the gate of the keeper transistor. Thus keeper transistor will turn on to keep the dynamic node high, fighting the effects of leakage.

C. Controlled Keeper by Current Comparison Domino logic (CKCCD)

A new circuit design with Controlled Keeper by Current Comparison Domino (CKCCD) is proposed to make the domino circuits more robust and with low leakage without significant performance degradation or increased power consumption. The reference current is compared with the pull down network current. If there is no conducting path from dynamic node to ground and only current in the PDN is the leakage current.

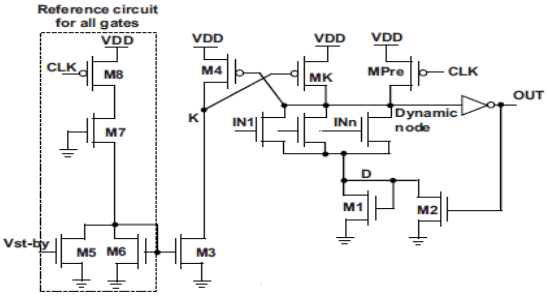

Figure 7. Controlled keeper by Current Comparison Domino

This idea is conceptually illustrated in figure 7. In fact there is a race between the pull down network and the reference current

D. Current Comparison Domino (CCD)

In the CCD circuit, the current of the PUN is mirrored by transistor M2 and compared with the reference current, which replicates the leakage current of the PUN. The topology of the keeper transistors and the reference circuit, which is shared for all gates, which successfully tracked the process, voltage and temperature variations. The CCD circuit employs pMOS transistors to implement logical function, as shown in figure 8. This circuit is similar to a Replica Leakage Circuit, in which a series diode-connection transistor *M*6 similar to *M*1 is added. Using the N-well process, source and body terminals of the pMOS transistors can be connected together such that the body effect is eliminated. By this means, the threshold voltage of transistors is only varied due to the process variation and not the body effect. Moreover, utilizing

pMOS transistors instead of nMOS ones in the N-well process, it is possible to prevent increasing the threshold voltage due to the body effect in existence of a voltage drop due to the diode configuration of transistor M1, yielding decreasing the delay.

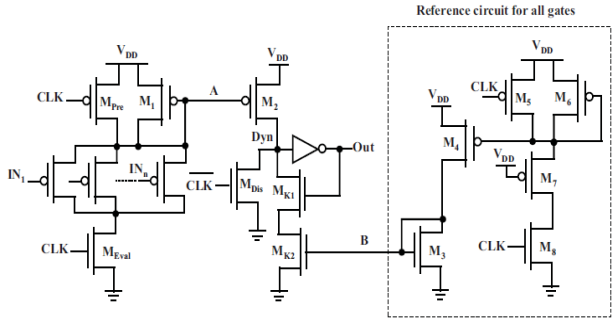

Figure 8. Current Comparison Domino

III. PROPOSED DESIGN

Since in wide fan-in gates, the capacitance of the dynamic node is large, speed is decreased dramatically. In addition, noise immunity of the gate is reduced due to many parallel leaky paths in wide gates. Although the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention [14]. A Leakage Current Replica (LCR) keeper for dynamic domino gates that uses an analog current mirror to replicate the leakage current of a dynamic gate pull-down stack and thus tracks process, voltage, and temperature. The proposed keeper has an overhead of one field-effect transistor per gate plus a portion of a shared current mirror [7].

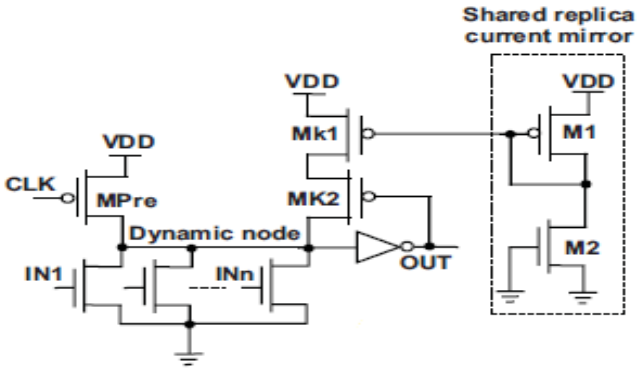

Figure 9. Proposed LCR keeper

The proposed leakage resistant domino uses a current mirror and PMOS as well as NMOS transistors to conquer the leakage produced by the circuit. Current mirror is a cost-efficient resistor that refuses leakage and can be shared among all gates [9]. A current mirror is an element with at least three terminals. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name current mirror. A current mirror reads a current entering in a read-node and mirror this current (with a suitable gain factor) to an output node (nodes). Under ideal conditions, the current mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals.

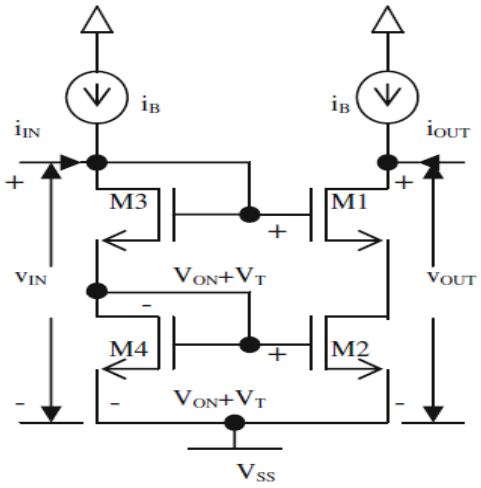

Figure 10. Current mirror

IV. SIMULATION RESULT

The simulation is done for the proposed scheme with the fan-in range of 8,16,32,64 bit OR gate design. The circuit power is evaluated by using the 350nm technology with 5v supply. It uses 10MHz as an operating frequency. The OR gate designed using LCR keeper. Because this technique uses less number of transistor when compared to the other methods. The LCR keeper uses a conventional analog current mirror that tracks any process corner as well as voltage and temperature. The figure 11 shows the schematic design for proposed LCR keeper using OR gate and figure 12 shows the waveform for the proposed LCR method.

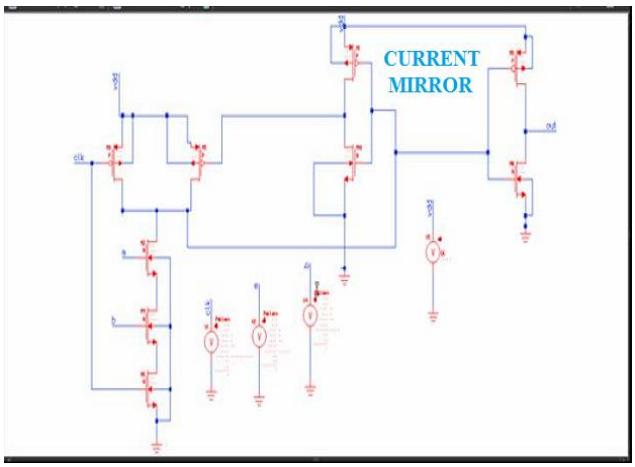

Figure 11. Schematic for proposed LCR method

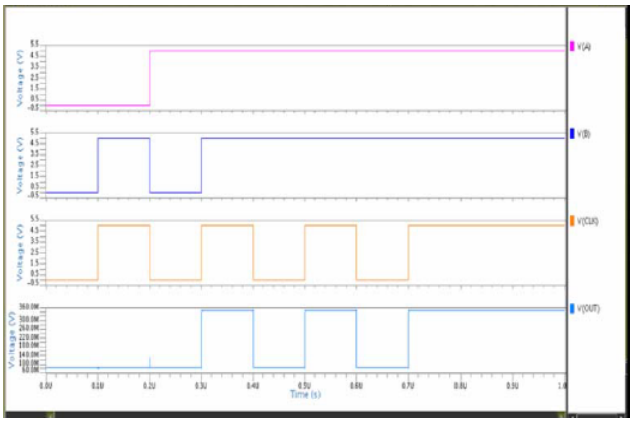

Figure 12. Waveforms for proposedd LCR method

In the 8-bit, only 8 transistors are used in Pull-Down network, hence it produces less leakage current. The stacking of NMOS keeper may reduce the leakage power. But the power consumption of those transistors are dominant than the leakage power reduced by that transistors. This procedure is to be continued for 16-bit gates.

The current mirror circuit is simulated using theEldo simulation file and the layout is obtained using the same.

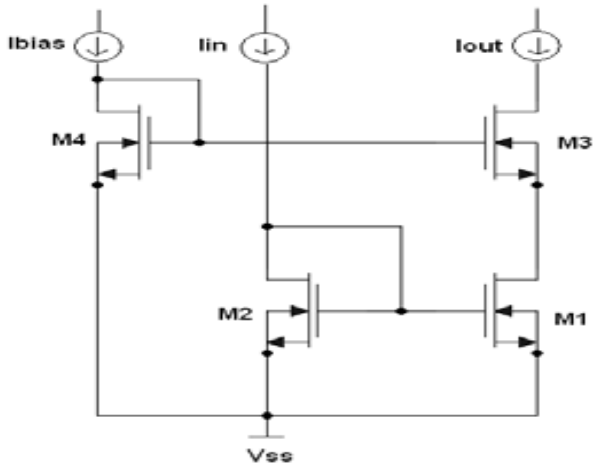

Figure 13. Schematic of analog current mirror

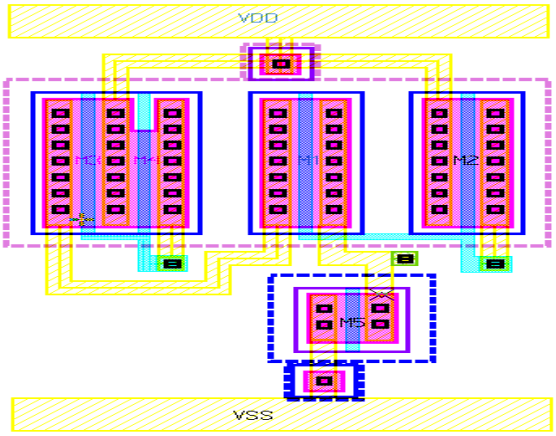

Figure 14. layout of current mirror

The transistor aspect ratio of the above current mirror circuit is given as Table 1,

TABLE I. TRANSISTOR ASPECT RATIO

Transistors	W(µm)	L(µm)
M1-M2-M3	22/0.2=110	1
M4	8/0.2=40	1

Normally in domino logic, in the Pull up network, we use only one PMOS transistor instead of ‘n’ transistor n=4,8&16 etc., and the logic will be implemented with the pull down network. By reducing the number of transistors, capacitance decreases. Few transistors means limited switching (charging and Discharging) of the capacitor. So dynamic power consumption gets decreased since the main source for dynamic power dissipation is charging and discharging.

As known already leakage current occurs due to unwanted current flow between source and the drain of a transistor. This leakage current can be avoided by the “stacking effect”. Stacking effect says that when two or more transistors in series are at off condition, the leakage current can be reduced.

V. CONCLUSION

A continuous scaling of CMOS technology, effective management of leakage power is a great challenge. Thus, new designs were necessary to obtain desired noise robustness in very wide fan-in circuits. Moreover, increasing the fan-in not only reduced the worst case delay, it also increased the contention between the keeper transistor and the evaluation network. The IRTS report state that leakage power dissipation may exceed dynamic power dissipation at the 65nm and fore coming technologies. The proposed technique uses an analog current mirror circuit and it is based on comparison of mirrored current of the pull-up network with its worst case leakage current. It replicates the leakage current of a dynamic gate pull-down stack and it tracks the process, voltage and temperature using the stacking effect. It

improves the performance of the current mirror circuit which will reduce the leakage current. The switching activity of the capacitor is limited by reducing the number of transistors.

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