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# Low Power VLSI Circuit Design and high performance using lector approach at 90 nm Technology

Umesh J Chavan
Department of Electronics and Communication Engg
PDA College of Engineering Kalaburagi, India
umeshchavan100@gmail.com

Siddarama R.Patil
Department of Electronics and Communication Engg
PDA College of Engineering Kalaburagi, India
pdapatil@gmail.com

***Abstract*— Many a change have been taking place in the technologies and trends in very large scale integration (VLSI) these days. The main factors in VLSI are Area, Speed and power. As there is a need of low power circuits in all real time applications like consumer electronics, medical applications, and mobile applications. So low power design theme is raised. As this paper introduces a method to reduce power dissipation in digital CMOS circuits using Lector approach. VLSI circuit designs are growing towards widespread attention due to the requirements of minimum energy consuming. Leakage energy and propagation delay is a considerable part of the overall energy dissipated in the VLSI circuits. This lector approach deals with the two parameters and analysis is done for save energy leakage VLSI circuits low power systems by the use of lector approach implementations. To overcome by leakage power reduction more efficient approach is lector at 90nm technology provides more efficiency and high performance [1]. EDA tanner tool is used to simulation.**

Keywords— ***Sub-threshold, Voltage Scaling; lector Approach, conventional; Power Delay Product*; Very Large Scale Integrated (VLSI) Circuits;**

## I INTRODUCTION

To achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially. High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. The main factor in the leakage power is the sub-threshold leakage current which increases as the channel length of the MOSFET decreases [2]. Thus to achieve low power performance, lowering the supply voltage is the most effective way as the dynamic power varies as the square of supply voltage and the leakage power varies linearly with supply voltage. But it results in drastic degradation of performance by reducing the supply voltage and keeping the threshold voltage at its original value, because as the supply voltage is reduced the gate drive voltage (VDD-VT) reduces and thus the delay increases, since propagation delay in a CMOS gate is Approximated as[3]

$$T_d = ($$ ----1

Where α is small positive constant used to that models the short Channel effects. To overcome the performance degradation, threshold voltage (VT) is to be reduced. Reduction in threshold voltage causes an exponential increase in sub-threshold leakage current, thereby static power. As one continues to scale down supply voltage and threshold voltage, the increased leakage power can dominate the dynamic switching power [4].

## II. RELATED WORK

There are numerous methods proposed to control leakage power dissipation. Power gating is one of the techniques proposed for leakage reduction, which turns off the device by cutting OFF the supply voltage. In this technique bulky NMOS and/or PMOS device called sleep transistor is used in a path between supply voltage and ground. This is done to create virtual power and ground rails in the circuit. This technique creates a negative effect on the circuit switching speed when the circuit is operating in active mode. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately. This additional hardware consumes power throughout the circuit

operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors [5].

A technique makes use of the dependence of the leakage current on the input vector to the gate. With additional control logic, the circuit is put into a low-leakage standby state when it is idle and restored to the original state when reactivated. Reactivation state forces the need to remember the original state information before going to low-leakage standby state. This requires special latches, thereby increasing the area of the circuit by about five times in the worst case. Also, the amount of time for which the unit Remains in idle state should be long enough so that the dynamic power consumed in forcing the circuit to low leakage state and the leakage power dissipated in the standby state together is less than the leakage power without the technique. The use of multiple threshold voltage CMOS (MTCMOS) technology for leakage control is another technique [6]. The transistors of the gates are at low threshold voltage and the ground is connected to the gate through a high-threshold voltage NMOS gating transistor. The logical function of a gating transistor is similar to that of a sleep transistor. The existence of reverse conduction paths tend to reduce the noise margin or in the worst case may result in complete failure of the gate. Moreover, there is a performance penalty since high-threshold transistors appear in series with all the switching current paths. A variation of MTCMOS technique is the Dual VT technique, which uses transistors with two different threshold voltages. Low-threshold transistors are used for the gates on the critical path and high-threshold transistors are used for those not in the critical path. In both MTCMOS and Dual VT methods, additional mask layers for each value of threshold voltage are required for fabricating the transistors selectively according to their assigned threshold voltage values. This makes the fabrication process complex. The techniques discussed above suffer from turning-on latency, that is, when the idle subsections of the circuit are reactivated, they cannot be used immediately because some time is needed before the sub-circuit returns to its normal operating condition. The latency for power gating is typically a few cycles, and for Dual VT technology, is much higher. Also, these techniques are not effective in controlling the leakage power when the circuit is in active state. Forced stacking introduces an additional transistor for every input of the gate in both N- and P-networks [7]. This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current. However, the loading requirement for each input introduced by the forced stacking reduces the drive current of the gate significantly This results in a detrimental impact on the speed of the circuit. The sleepy stack technique has a structure merging the forced stack technique and the sleep transistor technique. When applying the sleepy stack technique, each existing transistor is replaced with two half sized transistors and add one extra sleep transistor. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high-$V_{th}$ transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is drastically increased area. And the major disadvantage of having controlling circuitry for sleep transistors is also carried here. As the sleep transistors are bulky, hence increases the dynamic power. Sleepy Keeper is a better leakage reduction technique compared to sleepy stack. It gives an excellent alternate for sleepy stack in terms of reducing the area overhead since it doesn't need three transistors to be replaced to one transistor. Sleep transistors are connected to the circuit along with NMOS connected to $V_{dd}$ and PMOS connected to Gnd [8]. The sleep transistor is turned on when the circuit is active and turned off when the circuit is in idle state with the help of sleep signal. This creates virtual power and ground rails in the circuit. Hence, there is a significant detrimental effect on the switching speed when the circuit is active. The identification of the idle regions of the

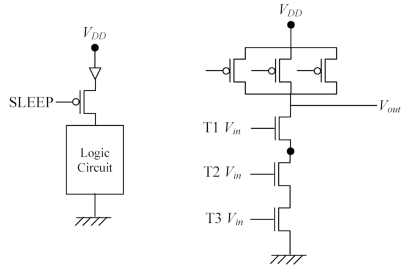


**Fig. 1 Nand gate circuits for Conventional approach**

Conventional type approach is efficient for nand gate but all there are limitation. Three T1,T2 and T3 CMOS and PMOS transistor is used to designed that is shown in figure .1 Circuit and the generation of the sleep signal needs an additional hardware capable of predicting the circuit states accurately, thereby increasing the area requirement of the circuit. This technique creates a negative effect when the circuit is operating in active mode in terms of the circuit performance. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep [9].

## III. LECTOR TECHNIQUE

LECTOR approach for reduction of leakage power is based on the effective stacking of transistors in the path from supply voltage to ground. The basic idea behind LECTOR is

based on the concept that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In this method, two leakage control transistors (LCTs) were introduced in each CMOS gate, a PMOS (LCT1) added to the pull-up network and a NMOS (LCT2) added to the pull-down network and the gate terminal of one LCT is controlled by the source terminal of the other, such that one of the LCTs is always *near its cutoff* region of operation for any input(s) given to the CMOS gate, thus providing additional resistance in the path from supply to ground, decreasing the sub-threshold leakage current, thereby the static power. This section illustrates Leakage Control TransistOR (LECTOR) technique with the case of memory circuits and other [10].

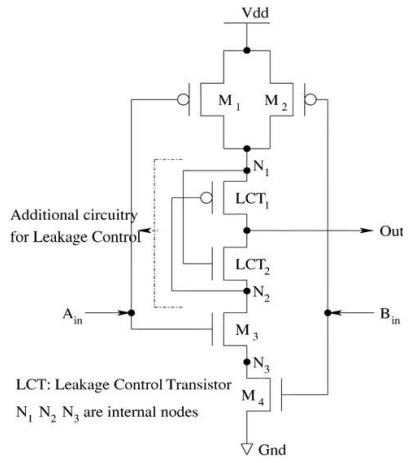


**Fig.2 . LECTOR based NAND Gate**

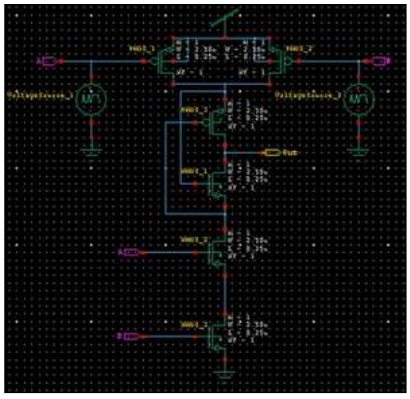

**Fig. 3 . LECTOR based NAND Gate**

A CMOS NAND gate with the addition of two leakage control transistors which is known as LECTOR NAND is shown in Fig. 1. Two leakage control transistors LCT1 (PMOS) and LCT2 (NMOS) are introduced between the nodes N1and N2 of the pull-up and pull-down logic of the NAND gate. The drain nodes of the transistors LCT1 and LCT2 are connected together to form the output node of the NAND gate. The source nodes of the transistors are connected to nodes N1 and N2 of pull-up and pull-down logic, respectively. The switching of transistors LCT1 and LCT2 are controlled by the voltage potentials at nodes N2 and N1 respectively. This wiring configuration ensures that one of the LCTs is always *near its cutoff region*, irrespective of the input vector applied to the NAND gate. This can be seen from the dc characteristics

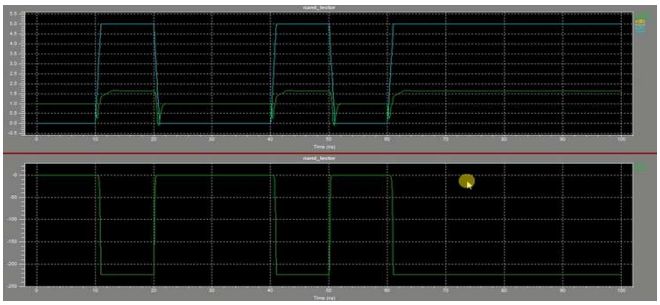

**Fig. 4. LECTOR based NAND Gate Waveform from EDA Tanner**

**Table.1 Results and Discussion**

| Technology | Circuit | Conventional approach (nm) | Lector approach(nm) |
|---|---|---|---|
| 90nm | Inverter | 5.08125e-008 | 2.08125e-008 |
| | Nand gate | 6.525e-008 | 6.35374e-008 |
| 90nm | Nor gate | 7.7250e-008 | 5.101e-008 |

Table.1 shows the static power consumption of the CMOS inverter circuit. Proposed CMOS inverter, nand, nor circuit dissipates less power compared to the other two circuits. The total power dissipated by CMOS inverter, 2-input NAND and NOR gates Lector approach less power compared to conventional circuits. CMOS inverter dissipates less power compared to the corresponding circuits designed using LECTOR technique. Static power consumed by NAND and NOR gates designed using conventional, LECTOR and proposed circuit techniques is summarized in fig.3. We have listed the leakage power dissipated during each possible input vector. In the table, 'A' and 'B' represents the inputs to the gate. Power-Delay-Product (PDP) is the important parameter to assess the quality and performance of logic circuits. It represents the energy consumed for switching event. It is referred to have the least value of PDP for the logic circuits. We measured PDP for the all three designs (conventional, LECTOR and proposed) and summarized in fig.2. CMOS inverter circuit along with the two logic gates NAND and NOR designed with proposed technique results in less PDP compared with the conventional design. Proposed CMOS inverter exhibits less PDP compared to the CMOS inverter circuit designed through LECTOR approach as a graphic and insert it into the text after your paper is styled.

## CONCLUSION

This paper briefly implemented the two techniques for power reduction at circuit and operation of system level and general state-of-the-art system -level low power techniques are evaluated. The paper gives the how the leakages take place in Conventional method and how the power dissipation can be reduced. Using Lector approach. The power measurement is done two parameters leakage (dissipation) and propagation delay between transistors, these results assures the minimum leakage compared to the conventional approach. We observed and considered Nand gate circuit design, and Hence Lector approach result is efficient.

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