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Low-Power Dual Active Revolutionize Flip-Flop Using Clock gating technology

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***Abstract*— Reducing power consumption in very large scale integrated circuits (VLSI) design has become an interesting research area. Most of the portable devices available in the market are battery driven. These devices impose tight constraint on the power dissipation. Reducing power consumption in such devices can be improve using clock gating technique..The proposed designs eliminate the large capacitance present in the precharge node of several designs by following a split dynamic node structure to separately drive the output pull-up and pull- down transistors.The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power and speed efficient method to incorporate complex logic functions into the flip-flop. Also DDFF and DDFF-ELM are compared with other designs by implementing a 4-b Johnson up-down counter. The performance improvements indicate that the proposed designs are well suited for modern high-performance designs where power consumption is of major concern.By applying clock gating technique get high throughout in low power.**

***Index Terms* —Dynamic Flip-flop,Gated clock,Low power design,Johnson counter.**

1 INTRODUCTION

Technology and speed are always moving forward from low scale integration to large scale integration i.e from megahertz to gigahertz. The system require-ments are also rising up with this continuous advancing process of technology and speed of operation. In synchro- nous systems, high speed has been achieved using advanced pipelining techniques. In modern deep-pipelined architectures, pushing the speed further up demands a lower pipeline over- head. This overhead is the latency associated with the pipeline elements such as flip-flops and latches.

1.1 FLIP-FLOP

The flip-flop or latch is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. Flip-flops and latches are used as data storage elements. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state.

Semi-static and Dynamic Flip-Flops:

Static (Non-precharged) Flip-Flop: a cascaded pair of static latches clocked in a complementary style.Semi static Flip-Flop: a cascaded pair of static and dynamic latches clocked in a complementary style.Fully dynamic Flip-Flop: a cascaded pair of dynamic latches clocked in a complementary style.Differential Flip-Flop: a cascaded pair of a static, dynamic or mix of differential latches clocked in a complementary style.

1.2 LATCHES

A Static Latch:

A cross-coupled inverter pair produces a bistable element. The bistable states are used to memorize binary data as long as the supply voltage exists.Another signal(s) (Clock) is/are used to allow transparency or no-transparency between the I/P and O/P of the bistable element

A Dynamic Latch:

Temporary storage of a charge in the parasitic capacitors of a circuit that is periodically refreshed . The stored charge is used to memorize binary data.The advantages of using latches or flipflop leads to

Lowest power supply voltage.Smallest geometry, highest frequency device operating them at lowest possible frequency.Using parallelism and pipelining to lower required frequency operation.Power management by disconnecting the power source when the system is idle. Designing the system to have lowest requirement on subsystem performance for the given user level functionality.

2 LITERATURE SURVEY

Various types of flip-flops have been used . However there is still scope for improvement in them particularly in their area and power consumption.

The Semidynamic flipflop reduces the pipeline overhead, since each flipflop can be viewed as a special logic gate that serves as a synchronization element. High performance at moderate power consumption. Due to variability, the setup time of some of the flip-flops samples is violated and these samples malfunction reducing the functional yield.

The existing Cross charge control flipflop reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors.XCFF has a comparatively lower CLK driving load. The main drawback is that the redundant precharge at node X2 and X1 for data patterns containing more 0 s and 1 s.The large hold time requirement resulting from the conditional shutoff mechanism.Effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design.

The proposed design DDFF DDFF is to reduce pipeline overhead Pipeline elements such as the flip-flops and latches.DDFF offers unconditional mechanism. Reset function has been used in DDFF.This has less power dissipation.Use least no of devices & less area.Due to small precharge node,clock & data input makes power efficient.The main advantage of DDFF is elimination of charge sharing.

The advanced DDFF-ELM performs the function of a flip-flop when no logic is embedded, its performance as a flip-flop is compared with other flip-flops along with DDFF. The CLK driving power is found as the difference between power dissipated in the inverter (INVCLK) when loaded with the flip-flop and when not loaded with the flip-flop. It gives 29%,10%, and 7% reduction in total power dissipation compared to SDFF, PowerPC, and XCFF. Comparable to CDMFF providing 8% improvement in PDP.

Finally the power dissipation of the 4-b Johnson up-down counter designed with multiplexer-embedded flip-flops. The CLK driving power and the internal power dissipation are also provided in order to highlight the performance improvement. About 33% of the CLK power dissipated in SDFF can be saved using the proposed design, and it dissipated 27% less in total power.

3 SYSTEM ANALYSIS

The techniques used in existing system are to reduce the charge sharing. Reducing this charge sharing has a profound effect in reducing the power dissipation .Flip-flops can be categorized in different ways:

Semi-Dynamic Flip-Flop is One of the fastest flip-flops structures.The most convenient structure for high performance applications.High performance at moderate power consumption.Represents a compromise between the MS-FF and the Pulsed-FF topologies.Uses differential pair architecture.This can beimplemented in the high performance WD21264 Alpha processor**.**

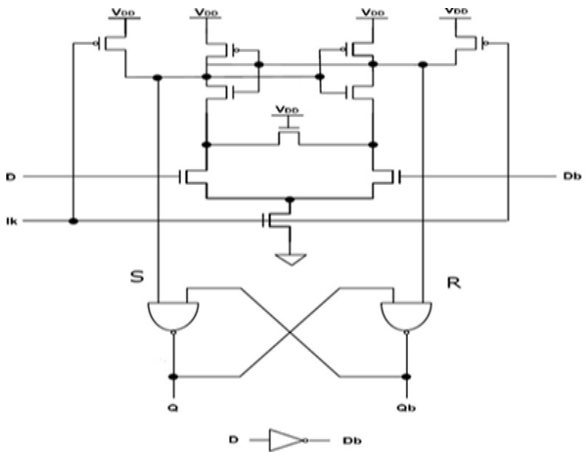


Fig3.1 Block representation of Semidynamic flipflop

Hybrid flipflop has the features

Single phase clock.Edge triggered, on one clock edge

The Hybrid latch has the features like

Soft clock edge property.It have brief transparency, equal to 3 inverter delays.Also negative setup time.It allows slack passing and absorbs skew.

Hold time is comparable to HLFF delayminimum delay between flip-flops must be controlled.Fully static and possible to incorporate logic.Soft Edge Property Also known as cycle borrowing or slack passing.

4 MODULE DESCRIPTION

4.1 Semidynamic flip-flop

Semidynamic circuits that internally have a precharge and evaluation phase similar to dynamic gates. The main features of the basic design are short latency, small clock load, small area and a single-phase clock scheme. Furthermore this flip-flop family has the capability of easily incorporating logic functions with a small delay penalty.

This feature greatly reduces the pipeline overhead since each flipflop can be viewed as a special logic gate that serves as a synchronization element. High performance at moderate power consumption.

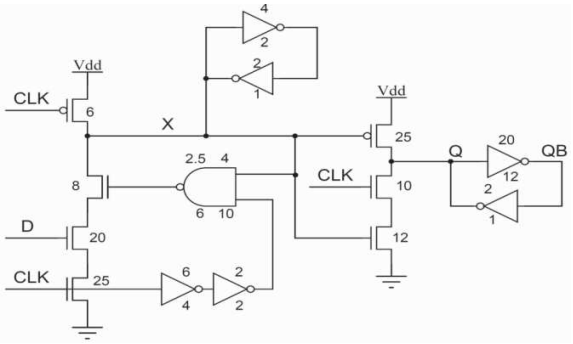


Fig 4.1 Block diagram for Semidynamic flipflop

4.2 Cross charge control flip-flop

Cross charge control flipflop has large precharge capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this precharge node. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF. It reduces the power

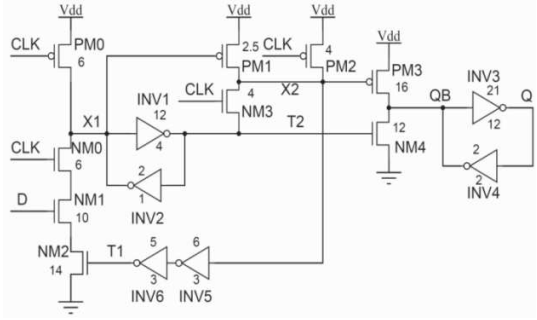


Fig 4.2 Block diagram for Cross charge control flipflop

In addition to the large hold time requirement resulting from the conditional shutoff mechanism a low to high transition in the CLK when the data is held low can cause charge sharing at node X1. This can trigger erroneous transition at the output unless the inverter pair INV1-2 is carefully skewed. This effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design. X2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF.

4.3 Proposed DDFF

The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2)the precharge phase, when CLK is low. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If D is high prior to this overlap period, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through NM4. The low level at the node X1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs.

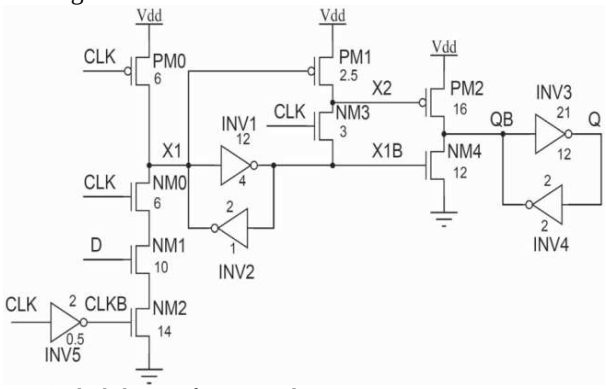


Fig 4.3 Block diagram for Proposed DDFF

Thus node X2 is held high by the pMOS transistor PM1. As the CLK falls low, the circuit enters the precharge phase and node X1 is pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If D is zero prior to the overlap period, node X1 remains high and node X2 is pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge.

4.4 Proposed DDFF-ELM

The revised structure of the proposed the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. Low to high transition of CLKB occurs when CLK is low, the node X1is held high by PM0 making this design free from charge sharing. The operation of the logic element is similar to the proposed DDFF.

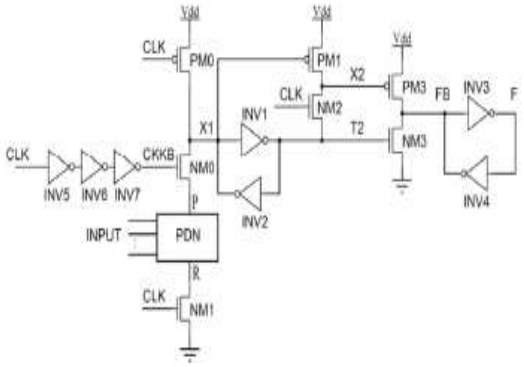


Fig 4.4 Block diagram for Proposed DDFF-ELM

4.5 JOHNSON COUNTER

A Johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage.The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely. These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using D- or JK-type flip-flops. A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. The main advantage of the Johnson counter counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD.To initialize the operation of the Johnson counter, it is necessary to reset all flip-flops, as shown in the figure.

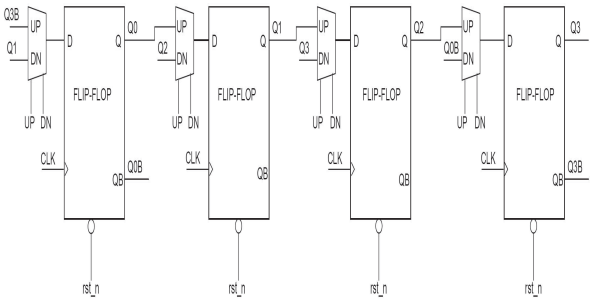


Fig 4.5 Block diagram for Johnson counter

4.6 Clock gating technique

Reducing power consumption in very large scale integrated circuits (VLSI) design has become an interesting research area. Most of the portable devices available in the market are battery driven. These devices impose tight constraint on the power dissipation. Reducing power consumption in such devices can be improve using clock gating technique.

Portable devices like mobiles, iPods, and laptops consume more energy which can exhaust battery charge within a short duration. Most of the power dissipation is of the dynamic type which necessities the reduction in switching power dissipation. This power dissipation occurs due to large power consumption.

In portable devices there is an opportunity for switching of a part of circuit that is not in use for a certain time. This results in the reduction in dynamic power dissipation of the device there by reducing overall power. Clock gating is the technique in which part of the design can be gated, that is registers that don't change their state are not given clock signals. By this technique the power consumption in storing the same bit to memory of the flip-flop is reduced. There

are different types in which the clock gating can be applied to a design. System level, combinational clock gating and sequential clock gating.

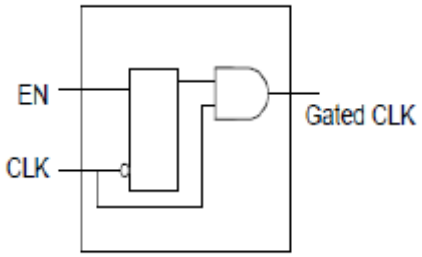


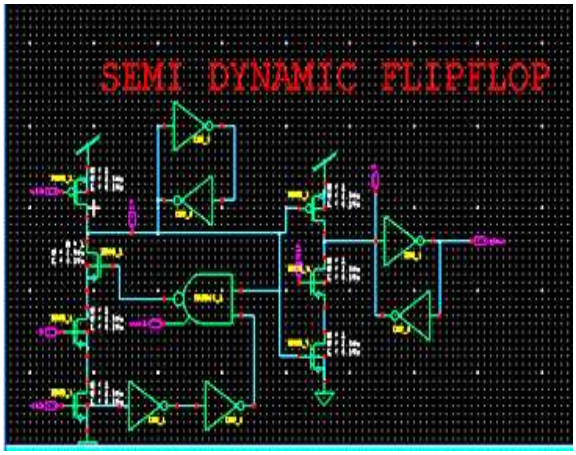
Fig 4.6 Block diagram for clock gating

The conditions for clock gating a design is: It should have a feedback system for registers, the enable signal activation logic of the mux should be determined, logic conditions that provide the output should be known. The gating elements are inserted according to the conditions where insertion of clock gating elements is possible and results in considerable power reduction. Power will be reduced when clock gating is applied to the design. The dynamic power obtained is overall power and not the gated power that is needed. This method is best suited for the design with millions of transistors. Clock-gating is a well-known technique to reduce clock power.

5 SIMULATION RESULTS

5.1 For Semi Dynamic flipflop

Circuit diagram



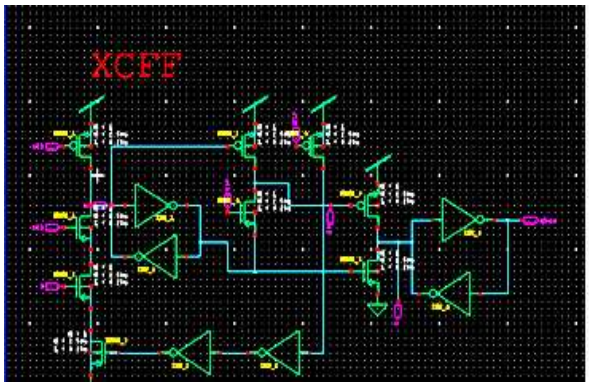
Output data

```
* BEGIN NON-GRAPHICAL DATA

Power Results
vdd from time 0 to 4e-007
Average power consumed -> 1.080822e-002 watts
Max power 7.890031e-002 at time 1.06113e-008
Min power 1.874678e-007 at time 1.3e-007


* END NON-GRAPHICAL DATA
*

* Parsing                          0.00 seconds
* Setup                            0.01 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.47 seconds
* Overhead                         1.58 seconds
* ----------------------------------------------
* Total                            2.06 seconds

* Simulation completed  with  6 Warnings

* End of T-Spice output file
```

This has the power consumption of 1.080822e^{-002}watts.

5.2 For Cross charge control flipflop

Circuit diagram



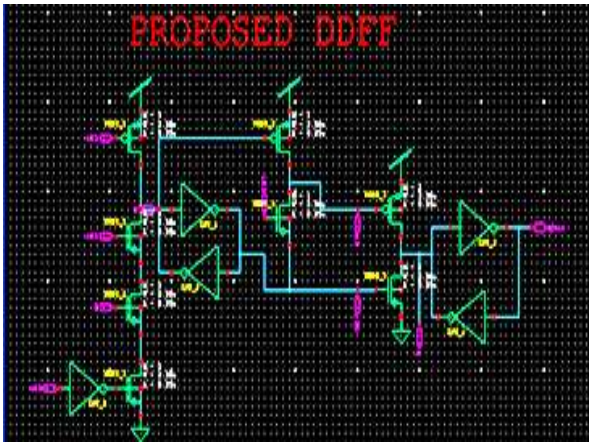
Output data

```
* BEGIN NON-GRAPHICAL DATA

Power Results
vdd from time 0 to 4e-007
Average power consumed -> 2.021335e-002 watts
Max power 7.014080e-002 at time 1e-009
Min power 1.418995e-007 at time 5.9e-007


* END NON-GRAPHICAL DATA
*

* Parsing                          0.00 seconds
* Setup                            0.01 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.22 seconds
* Overhead                         0.86 seconds
* ----------------------------------------------
* Total                            1.09 seconds

* Simulation completed  with  3 Warnings

* End of T-Spice output file
```

This has the power consumption of 2.021335e^{-002}watts

5.3 For Proposed DDFF flipflop

Circuit diagram



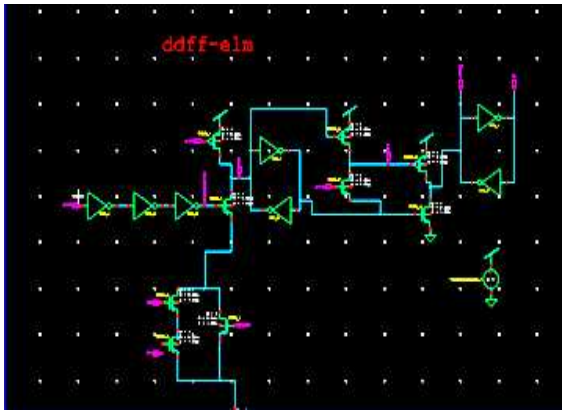
Output data

```
* BEGIN NON-GRAPHICAL DATA

Power Results
vdd from time 0 to 4e-007
Average power consumed -> 1.111672e-002 watts
Max power 4.182236e-002 at time 0
Min power 1.306964e-008 at time 1.28655e-007

* END NON-GRAPHICAL DATA
*

* Parsing                          0.00 seconds
* Setup                            0.01 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.20 seconds
* Overhead                         0.92 seconds
* ----------------------------------------------
* Total                            1.14 seconds
```

This has the power consumption of 1.111672e^{-002}watts

5.4 For Proposed DDFF-ELMflipflop

Circuit diagram



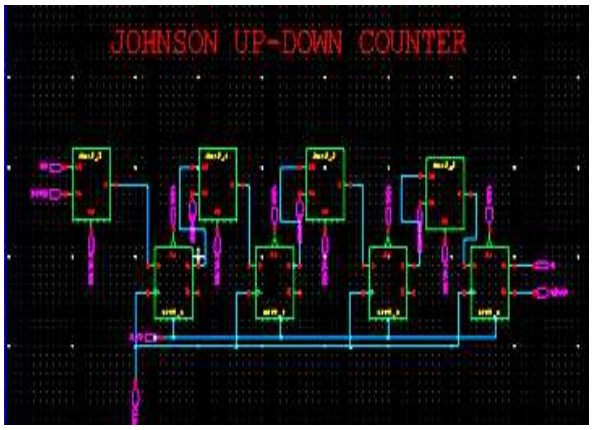
Output data

```
Power Results
vdd from time 0 to 4e-007
Average power consumed -> 1.024114e-002 watts
Max power 7.515783e-002 at time 1.05468e-008
Min power 1.339990e-003 at time 4.09611e-008

* END NON-GRAPHICAL DATA
*

* Parsing                          0.02 seconds
* Setup                            0.01 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.55 seconds
* Overhead                         1.80 seconds
* ----------------------------------------------
* Total                            2.37 seconds
```

This has the power consumption of 1.024114e^{-002}watts

5.5 For Proposed DDFF-ELM flipflop using Johnson counter

Circuit diagram



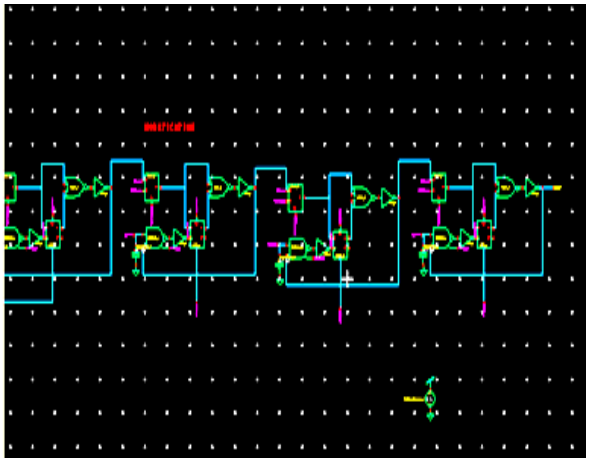
Output data

```
Power Results
vdd from time 0 to 4e-007
Average power consumed -> 8.306299e-004 watts
Max power 3.921108e-002 at time 4.075446e-008
Min power 4.366932e-010 at time 2.8464e-007

* END NON-GRAPHICAL DATA
*

* Parsing                          0.00 seconds
* Setup                            0.03 seconds
* DC operating point               0.03 seconds
* Transient Analysis               1.47 seconds
* Overhead                         1.41 seconds
* ----------------------------------------------
* Total                            2.94 seconds
```

This has the power consumption of $8.306299e^{-004}$watts

5.6 For proposed DDFF-ELM flipflop using Johnson counter using clock gating technique

Circuit diagram



Output data

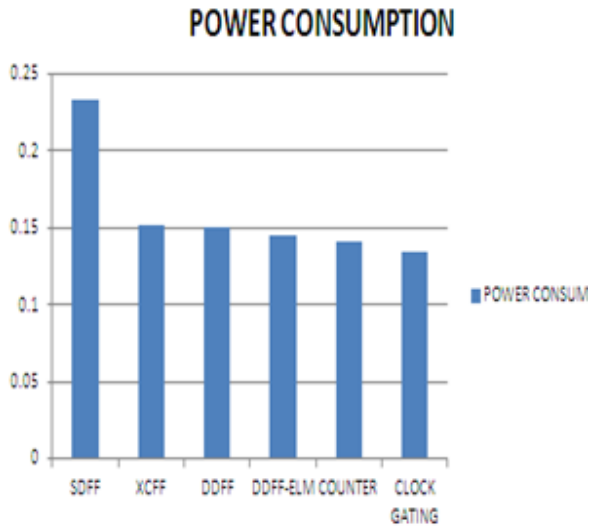
```
* BEGIN NON-GRAPHICAL DATA

Power Results
vdd from time 0 to 4e-007
Average power consumed -> 1.064250e-002 watts
Max power 1.741901e-001 at time 1.074906e-008
Min power 1.609054e-007 at time 1.8864e-007
```

This has the power consumption of $1.064250e^{-002}$watts

COMPARISION TABLE

FLIP-FLOPS	POWER CONSUMED FOR OPERATION(WATTS)
SDFF	**0.233557944**
XCFF	**0.152135173**
DDFF	**0.150448445**
DDFF-ELM	**0.145273351**
DDFF-ELM using counter	**0.140908758**
DDFF-ELM using clock gating technique	**0.134030575**

COMPARISION CHART



6 CONCLUSION

The proposed system eliminates the redundant power consumption present in the XCFF.A comparison of the proposed flip-flop with the conventional flip-flops showed that it exhibits lower power consumption along with comparable speed performances. By eliminating the charge sharing, the revised structure of the proposed technique is capable of efficiently incorporating complex logic in to the flip-flop.

It was proven that the proposed architectures are well suited for modern high-performance designs where area, delay-overhead, and power consumption are of major concern. It consumes low power .

Thus this idea includes how to improve the power consumption. Clock gating technique is proposed to reduce the power consumption of the circuit. The presented ELM out performs the SDFF in the CLK driving power and in internal power consumption. The efficiency of the flip-flop and the ELM were further highlighted using a 4-b Johnson up-down counter which would facilitate the advanced pipelining and enhance power consumption.

It reduce dynamic power consumption of sequential circuit is introduced. The proposed scheme is based on clock gating technique. And gate based clock gating is used in design example. Power calculation and simulation is performed using TANNER tool device. This result shows that clock gating technique significantly reduces the dynamic power consumption.

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