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DESIGN OF HIGH SPEED SPLIT SAR ADC WITH IMPROVED LINEARITY

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***Abstract*--Recently low power Analog to Digital Converters (ADCs) have been developed for many energy constrained applications such as wireless sensor networks and bio-medical applications. Successive approximation register (SAR) ADC are good candidates for low power applications and widely used for low energy application due to its minimum analog blocks. The static linearity performance in terms of the integral nonlinearity and differential nonlinearity and the parasitic effects of the split DAC, are analyzed. A code randomized calibration technique is done to correct the conversion nonlinearity in the conventional SAR ADC, which is verified by behavioral simulation. Here the SAR ADC is designed in such a way that the control module completely control the splitting up of modules and the speed of operation is changed using low level input bits. A dedicated multiplexer can be used to minimize the capacitor array structure. The control module controls the clock signal and determines the time at which the analog signal should enter the SAR logic. On attaining control over the time of arrival of input signals the speed of conversion can be increased and power utilization can be minimized.**

I. INTRODUCTION

Successive approximation registers Analog-to-digital converters are used as an alternative to the pipelined ADCs for battery-powered mobile applications, such as DVB-T, DVB-H and TDMB which require medium speed 10 MS/s–100 MS/s and medium-resolution. SAR ADCs achieve very low power consumption due to their simple structural design and operation. However, the SAR conversion relies basically on the arrangement of a capacitive DAC that subtracts the reference voltage from the input signal. The KT/C noise, capacitor mismatches, and parasitic of the split DAC affect the conversion precision.

The conversion nonlinearities, induced by supply noise, switching methods, and parasitic effects in SAR ADCs. The internal node parasitic in the split DAC is also analyzed, since it degrades the conversion linearity. This limitation can be fixed by a code-randomized digital calibration technique in order to improve the differential nonlinearity DNL and integral nonlinearity INL.

Prior to the binary DAC based techniques mentioned above, the authors reported a SAR ADC oriented digital error correction algorithm which required only the addition of a simple digital code with no DAC burden. This paper presents a speed-enhanced prototype SAR ADC that builds on this idea with advanced hardware implementation.

II. LITERATUTRE REVIEW

Dip. di Elettronica and Informazione e Bioingegneria, 2012

The optimal design of SAR ADCs requires the accurate estimate of nonlinearity and parasitic effects in the feedback charge-redistribution DAC. Since the effects of both mismatch and stray capacitances depend on the specific array topology, complex calculations, custom modeling and heavy simulations in common circuit design environments are often required. This paper presents a novel MATLAB-based numerical tool to assist the design of classic, split and with attenuation capacitor binary weighted capacitive array topologies with an even number of bits from 6 to 14.

Ho-Young Lee1 and Bumha Lee, 2012

Analog-to-digital conversion with a signal bandwidth of 10 to 20MHz and ENOB of 11 to 12b has become a common requirement in many modern wireless communication systems where low power consumption is always a necessity. This paper presents the design and the optimization of an asynchronous SAR ADC with attenuation capacitor achieving efficiency similar to conventional binary weighted array converters. Typically, the traditional 2-step pipelined ADC is not considered a good candidate to meet these design specifications, since it is implemented with a power hungry high-resolution flash sub-ADC and high-gain residue amplifier.

S. Saisundar and Shan Jiang, 2013

A 14-bit cyclic-pipelined Analog to digital converter (ADC) running at 1 MS/s. The architecture is based on a 1.5-bit per stage structure utilizing digital correction for each stage. The ADC consists of two 1.5-bit stages, one shift register delay line, and digital error correction logic. Inside each 1.5-bit stage, there is one gain-boosting op amp and two comparators. The circuit has an average power consumption of 3.5mA with 10MHz sampling clocks. The post-layout simulations of the design satisfy 12-bit SNDR with a full-scale sinusoid input.

Sang-Hyun Cho and Chang-Kyo Lee, 2010

A speed-enhanced 10b asynchronous SAR ADC with multistep addition-only digital error correction (ADEC) is presented in this paper. Three virtually divided sub DACs have a 0.5 LSB over-range between stages owing to additional decision phases incorporating DAC rearrange only. These redundancies make it possible to guarantee 10b linearity with a 37% speed enhancement under a 4b-accurate DAC settling condition at MSB decision. A prototype ADC was implemented in CMOS 0.13μm technology. The chip consumes 550μW and achieves a 50.6dB SNDR at 40MS/s under a 1.2V supply. The figure-of-merit (FOM) is 42fJ/conv-step.

EXISTING SYSTEM

The binary-weighted capacitive DAC is widely used in SAR ADCs. However the capacitance of the DAC array increases exponentially with the resolution, which imposes larger consumption of switching energy, area, and settling time. A valuable substitute is the split capacitive DAC, which has been recently reconsidered for medium resolution. Its key limitation lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity. However, by using the metal-insulator-metal (MIM) capacitor or/and DAC mismatch calibrations, the split structure can become suitable for a medium-resolution target. On the other hand, the conversion linearity is also directly correlated with the switching sequences of the DAC array where the conventional charge-redistribution switching results in worse conversion linearity and more energy losses. A V_{cm}-based switching technique has been recently proposed, which achieves a significant switching energy saving when compared with set-and-down and charge-recycling switching approaches.

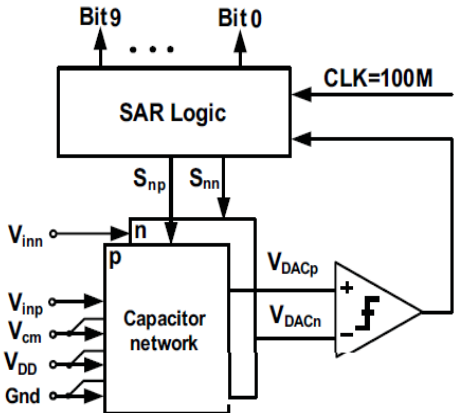

Fig.1 Block Diagram of ADC Architecture

III. PROBLEM STATEMENT

When supply voltage is used as reference voltage the switching power becomes dynamic which is correlated with the switching sequence. The diagram represents a conventional single-ended *n*-bit split DAC structure. During the global sampling phase the input signal represented as V_{in} is stored in the entire capacitor array. The algorithmic conversion then starts by switching only the MSB capacitor to *V*DD and the others to Gnd. The comparator output predicts the switching logic for the MSB capacitor. If Out results low S_m, k is switched back to Gnd. If Out_ {comp} becomes high, then S_m,k maintained *V*DD. Simultaneously, the S_m, k−1 switches to *V*DD for the next bit comparison. The above process repeats for $n - 1$ cycles. The conventional charge redistribution method is not effective in terms of power when discharging the MSB and charging the MSB/2 capacitor. The V_{cm} based switching method reduces the array capacitance to half resulting in 90% energy saving when compared with conventional method. The diagram represents the V_{cm} based switching algorithm. During the sampling phase voltage V_{in} gets stored in the capacitor array. During the conversion phase the bottom-plates of the capacitors gets switched to the V_{cm} first which raises the voltage −*V*in at the output.

DISADVANTAGE

The disadvantages of Split-SAR ADCs: Improved Linearity with Power and Speed Optimization are as follows:

- Superior conversion occurs due to the array's capacitors correlation during each bit cycling.
- Large switching transients are required which leads to insufficient DAC settling and supply ripples.
- Delay due to V_{cm}-based switching in DAC.

IV. PROPOSED SYSTEM

DESCRIPTION OF PROPOSED SYSTEM

A/D conversion is obtained with many algorithms. For obtaining power effectiveness, what often matters is not inventing new methods but finding the best use of known algorithms and achieving the optimum for the foreseen technology and the given specifications. High speed and medium-to-high resolution normally call for pipeline, two-step, or sub ranging schemes. The basic building blocks are the track-and hold, the comparator, and the op-amp. With medium resolution, the input track and hold is a source follower with passive sampling. Clock feed through is minimized with dummy elements and body effect is cancelled out by connecting the source and substrate. The power depends on the capacitive load that, in turn, is proportional to the number, N, of comparators served by the T&H. Since gm/CL is the relevant parameter power increases with the square of N. The power of the comparator depends on the resolution. For several tens of mV, just a latch makes the comparator. For resolutions from ten to few tens of mV, however, it is necessary to use a simple preamplifier before the latch.

ADVANTAGE

The advantages of the proposed system are as follows:

- It eliminates the errors and conventional switching.
- The reduction of switching power as well as the digital power from switching buffers.
- High accuracy.

PROPOSED SYSTEM ARCHITECTURE
CONFIGURABLE SPLIT SAR ADC

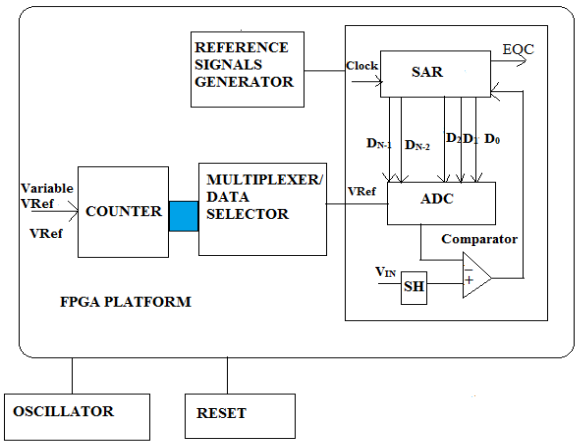

Fig.2 Split SAR ADC- Functional Block Diagram

V. FUNCTIONAL BLOCK DIAGRAM

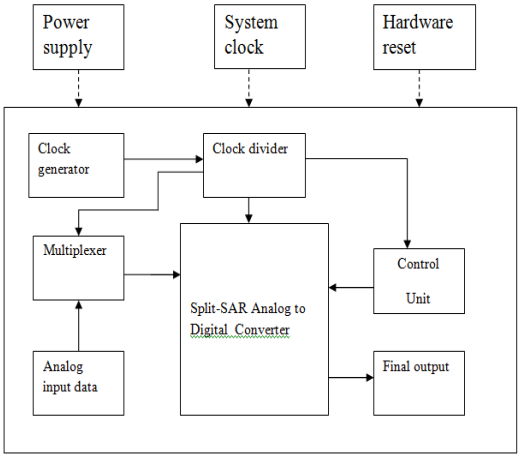

Fig. Functional Diagram of Proposed system

BLOCK DESCRIPTION OF PROPOSED SYSTEM

In the proposed system we are planning to implement SAR ADC in a configurable manner with different frequency inputs, the configurable means that the entire ADC architecture can work with different perfromance by changing the Vref of the ADC. Normally in all ADC Vref , Vin , Vth plays a major role in adc conversion by varying the values of Vref we can change the performance of the ADC.

SAR ADCs provide a high degree of configurability on both circuit level and architectural level. At architectural level the loop order and oversampling ratio can be changed, the number of included blocks, and way these blocks are arranged. At circuit level many things could change, such as bias currents, amplifier performance, quantizer resolution etc.

If an ADC is reconfigured in the way the blocks in the ADC are used and ordered, it is an architectural change of the ADC, or architectural reconfigurability. These blocks can also be changed, for instance how the amplifiers are biased, or how many bits of resolution that a quantizer has in a SAR ADC. These are examples of how circuit level reconfigurability is applied to an ADC.

VI. APPLICATIONS

RADIOSONDE

A radiosonde is French and German for probe is a piece of equipment used on weather balloons that measures various atmospheric parameters and transmits them to a fixed receiver. Radiosondes may operate at a radio frequency of 403 MHz or 1680 MHz and both types may be adjusted slightly higher or lower as required. A raw in sonde is a radiosonde that is designed to only measure wind speed and direction. Colloquially, raw in sondes are usually referred to as radiosondes.

MODERN RADIOSONDES MEASURE

- Pressure
- Altitude
- Geographical position (Latitude/Longitude)
- Temperature
- Relative humidity
- Wind (both wind speed and wind direction)
- Cosmic ray readings at high altitude

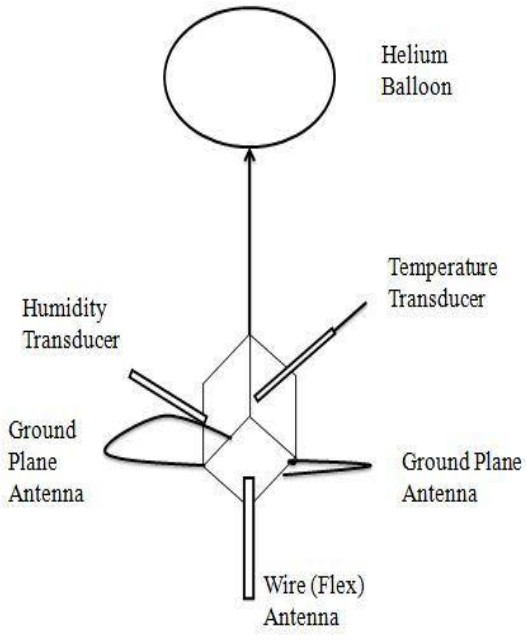

Fig. Radiosonde Measuring Ozone Concentration

VII. RESULT ANALYSIS

ASIG OUTPUT

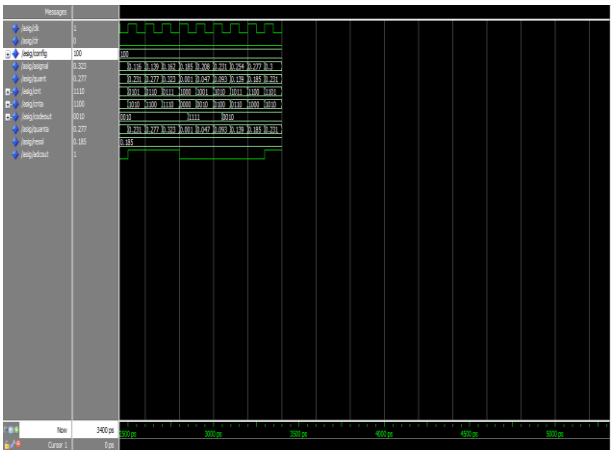

Fig.ASIG Output

APPLICATION OF SONDAE OUTPUT

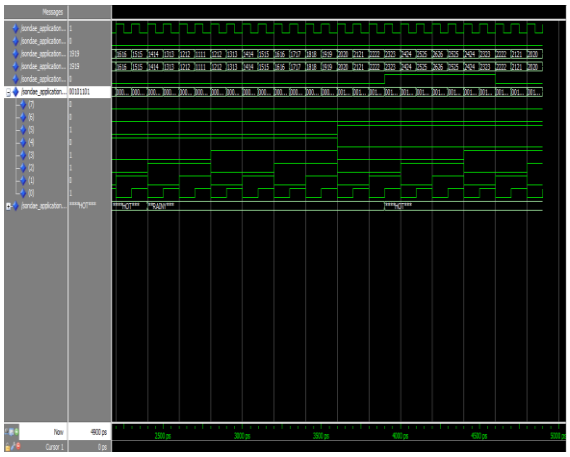

Fig.Application of SONDAE

INTEGRATION OUTPUT

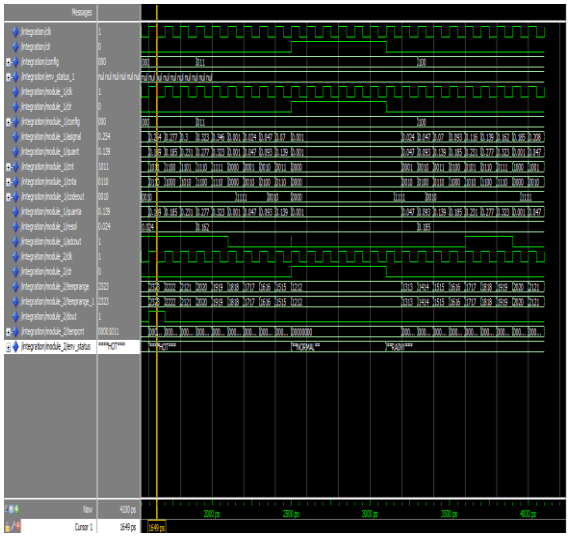

Fig.Integration Output

VIII. CONCLUSION

Two 1.2 V 10-b SAR ADCs operating at tens of MS/s with additional multiplexer was presented. The linearity behaviors of the DACs switching and structure were analyzed and verified by both simulated and measured results. According to an analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator is proposed in the circuit of a dual tail comparator. It has been designed adopting a binary weighted with attenuation capacitor array featuring a linearity and a total capacitance similar to a conventional binary weighted array but without requiring critical full-custom sub fF capacitors. The design and the layout of the array have been accurately optimized in order to reduce the parasitic capacitances at the top-plate node of the sub-DAC which degrade the linearity. This switching technique provides superior conversion linearity when compared with the conventional method because of its array's capacitors correlation during each bit cycling. The proposed code randomized calibration can eliminate the large DNL and INL errors during switching. Measured results demonstrated that both higher speed and lower power is achieved by using proposed SAR ADC architecture.

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