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PREDICTING HEART ATTACK USING LOW POWER ECG

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Abstract - Introduces **the concept, using a special collection of ECG features and a naive Bayes classification, of a fully integrated Electrocardiogram (ECG) signal processor (ESP). In the field of fiduciary points, real time and adaptive techniques were explored for the identification and delineation of the P-QRS-T waves. These methods are versatile with high sensitivity and accuracy in support to variations of the ECG signal. The MIT Physio Net and the American Heart Association used two databases of the heart signal recordings as a validation collection to test the processor's output. The overall classification accuracy was found to be 86 percent with the out-of-sample validation data with 3-size window centered on the application-specified integrated circuit (ASIC) simulation data. This paper analyses logical scale, area and energy usage using Xilinx in its proposed architecture. The architecture of the planned ESP was carried out by a CMOS procedure of 64nnanometres, with a surface area of 0,109m, 2m and a power consumption of 2.68 micro watts at a 10kg frequency and a working voltage of 1volt. It should be noted that the proposed ESP is the first ASIC implementation of an ECG-based processor to prevent a heart attack up to 3 hours before the beginning of the processor.**

Keywords—component, formatting, style, styling, insert

I. INTRODUCTION

ECG means electrocardiograph. Features and naive Bayes classification, of a fully integrated Electrocardiograph (ECG) signal processor (ESP) for prevision of ventricular arrhythmia. In order to draw fiduciary points, the real time and adaptive techniques were examined, for the detection and definition of the P-QRS-T waves. These techniques are robust with high sensitivity and accuracy for all variations in the ECG signal. The validation set was used to evaluate the performance of the processor through two databases with cardiac signal recordings from the MIT Physio Net and the American Heart Association. Integrated circuit simulation (ASIC) based on the application specified.

As a result, 86 percent of out-of-sample validation data with 3-s window size was found to be of overall classification accuracy. This paper analyses the logic size, area and power consumption using Xilinx in the proposed architecture.

The architecture of the proposed ESP was implemented using 64nanometers CMOS processes, which had an operating frequency of 10 kilo hertz, a voltage of 1 volt and a surface area of 0.109 mm, and consumed an output of 2.68 microwatts. The proposed ESP is an initial ASIC application for an ECG-based processor, which can be used up to 3 hours before starting a predictive heart attack.

Sudden heart death is the final result of ventricular arrhythmia, including ventricular tacti Cardia (VT), or ventricular fibrillation (VF), which represents nearly 300,000 lives each year in the United States. Ventricular arrhythmia is an irregular ECG which causes 75% – 85% of sudden deaths in people with heart failure unless it is treated in seconds. Most ventricular arrhythmia are exacerbated by cardiac dysfunction, hypertension, or cardiomyopathy and immediate mortality if not correctly diagnosed and handled. The ventricles have a rapid rhythm of over three consecutive beats at a pace of above 100 beats/min. VF is another rhythm marked by disorderly ventricle stimulation that allows blood pumping to stop automatically and further degenerates into a pulse less or smooth ECG predictor with no electrical heart operation.

The cardioverter defibrillator was found to be the best defense against accidental death in high risk individuals with ventricular arrhythmia. However, among people that do not have high risk profiles, more unexpected deaths occur. The standard condition for the diagnosis of ventricular arrhythmia is long-term ECG testing. The 12-lead ECG's are collected and tested to identify changes in the ECG signal characteristics.

II. EXISTING AND RELATED WORK

We people are not the only ones who wanted to create a device to prevent the heart attacks death rate, there were many seniors who did, the first idea of creating such device was came to a person in the early 1980's itself . But due to the lack of technology at that time the device was not completed but the team has done an extensive research and has passed don the records safely such a way the future people will be able to create the device.

In 2008 a group foreign people have created a device using ECG and CMOS to crate the predicting system , even though it was a success there were many complications for

using the device . One of which is its size was big, which is difficult to carry and the creation cost is very high.

In 2017 there was another team which tried to solve the same problem but they were using VLSI design, the end product of this project was a success , but it was consumption of power was very high and the accuracy is not that great either it was around
60 percent.

III. Specific Objective

We wanted to create a software with succeeding hardware to detect heart attack before it surfaced and to take precautions before. So we can save as many as lives possible.

IV. Proposed Block Diagram

This is the block diagram of the system which contains ECG Preprocessing, Feature Extraction and ECG Classification stages.

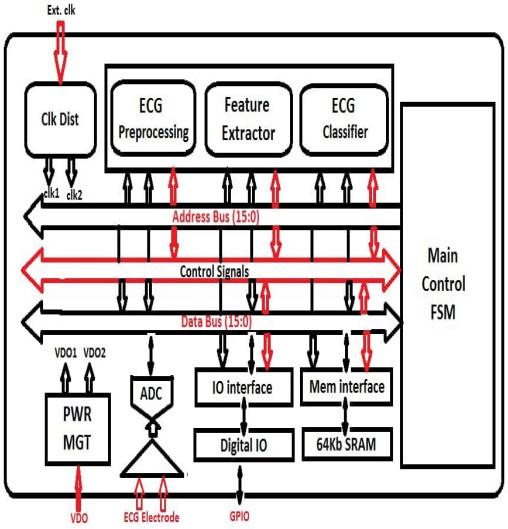


Fig 1. Block Diagram

The suggested ESP architecture is explained. The architecture comprises the three-stage modules alongside a principal FSM which controls the information flow between the various stadiums, as seen. The retrieval of the information is performed with a fixed point display. In the input processing level, the digital ECG data is used serially (from the test bench) with a resolution of 8 bits while a variable number of bits is used in separate steps, improving

precision and avoiding bumping errors. As seen, ried phases. The retrieval of the information is performed with a fixed point display. In order to enhance precision and prevent truncation errors, the digitized ECG data is applied serial (from the test bench) at the input to the preprocessing phase with a resolution of 8 bits.
Otherwise the waveform is reversed and the local minimum ECG signal is then the right top inside a corresponding window. For a bi phasic wave, the local limit should be both larger than the rim and, thus, the definite amount of the local minimum. The tactics monitor the start-up and offset values of the P-QRS-T surface waves, by finding samples such as the zero pitch of the ECG signal. Due to the starting point the sampling point with a zero pitch, which is previously at the height is defined. Similarly, on the other side of the height, the offset point is determined. But often there is a reversal of the initial symbol reflecting a false signal. The tactic applies a separate criteria to uncover this for a precise delimitation of the wave borders since the fiduciary points are always fused smoothly to the iso-electric side.
Due to the average value after removal of the QRS complex, the iso-electric line is observed. This definition is critical and can be combined with the zero slope, such that the fiduciary points are precisely and well-defined. The FSM as a whole showing the T and P wave delineation mechanism. The complexities and therefore precision are discussed in the course of this paper at a time equivalent. To do this, we have carried out statistics that are known to solve the easiest discriminatory ECG features that can sustain poor device complexity and precision in biomedical science.

VI. Methodology

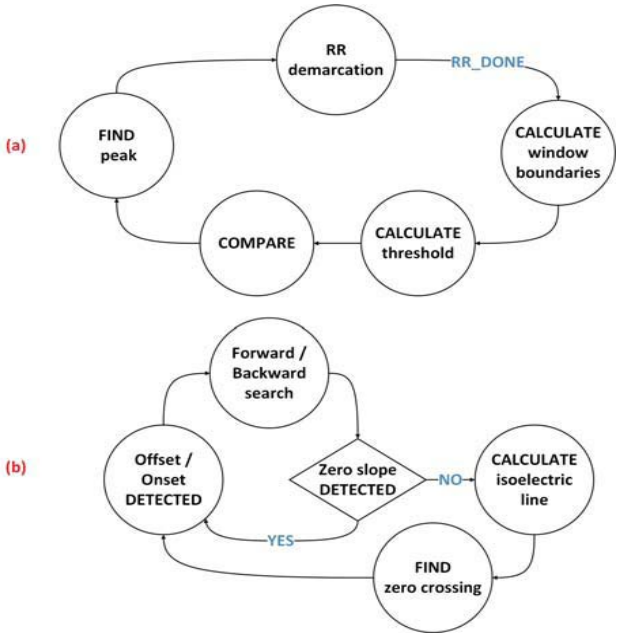


Fig 2. FSM of T and P wave delineation (a) Peak detection (b) Onset and offset delineation.

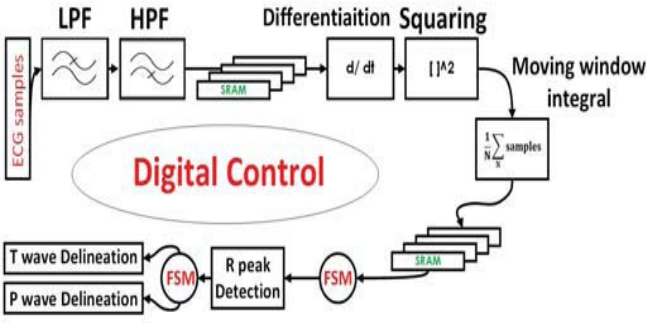


Fig 3. Preprocessing Stage

Preprocessing stage contains Filtering, QRS Detection, and P and T wave delineation.

A. ECG Filtering

The p reprocessing step is seen in above figure. Electrocardiogram filters are the first stage where the filter isolates prevalent QRS energy with LPF, HPF, SRAM and 10-Hertz sample, and attenuates P and T wave low frequency and high regular properties in relation to electrographic noise and power interference, respectively. Electrocardiogram signal filters are the first stage.

B. QRS Detection

QRS identification is the second phase of preprocessing. The Pan and Thompkins system detects the QRS complex. PAT is used around the world to measure the amplitude level, indicating that R summits are large in amplitude relative to others. This technique is used for the estimation of amplitude values. The filtering of the signal tactic is used to track R peaks with two intensities of any heartbeat.

C. P and T wave delineation

T and P wave delineation are the third step in preprocessing. For the delineation of T and P waves a new methodology is suggested. The adaptive scan window system along with the amplitude threshold distinguishes T and P peaks from the noise peak correctly. The QRS complex used as reference in each heartbeat for the detection of T and P waves in which two regions are labelled in relation to R peaks.

D. Feature Extraction Stage

The second step is the phase of extraction of functionality. The sophistication, and hence the precision of the feature extraction technique delivering the simplest outcome, are the two key parameters to remember when designing a prediction device detection. The findings of this analytics were obtained during a special series of ECG characteristics, which proved to be the main indicators of ventricular arrhythmia with simple timeline scheme and good precision of prediction. The features reflect these cycles on the ECG record like RR, PQ, QP, RT, TR PS and SP. These functions are taken from two successive heartbeats.

E. Classification Stage

The third step of the block diagram is the grading phase of the Naive Bayes Classifier. The naive Bayes classification framework can easily be built without any complex iterative parameter estimate which makes it especially useful for implementing hardware It assumes that all derived BCG characteristics have independently been evaluated and fucked up from the beginning with naive and efficient independent distributions between function vector. The classifier architecture is illustrated in figure.

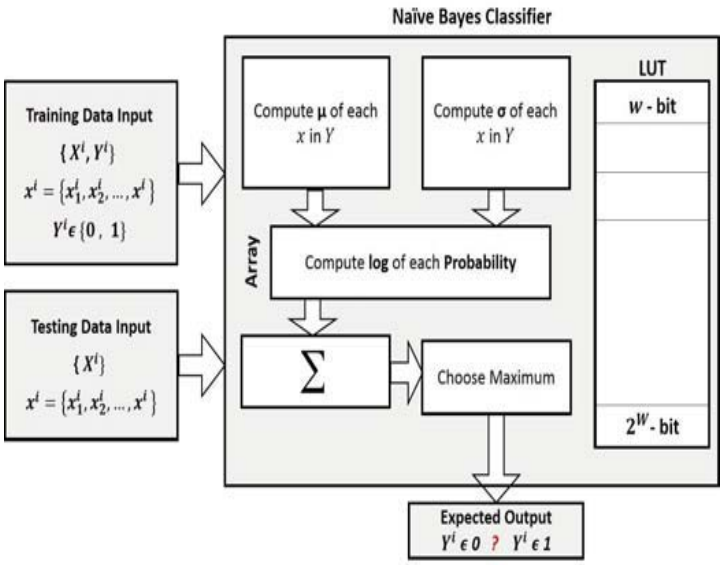


Fig 4. Architecture of Naive Bayes Classifier

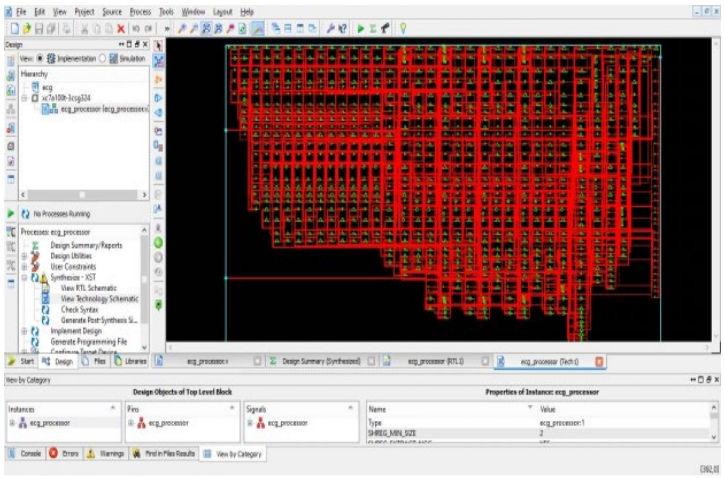
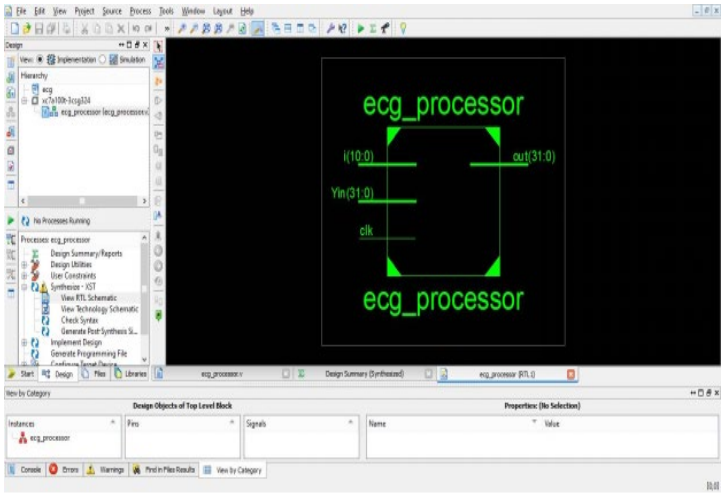
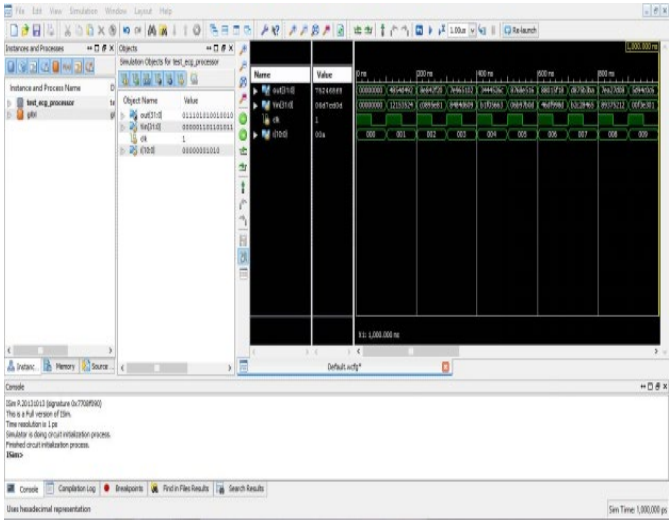


Fig 5. Schematic for ECG Preprocessor

VII. RESULTS





VIII. CONCLUSION

In this article a fully optimized digital ESP for ventricular arrhythmia prediction has been suggested, which blends a special range of ECG characteristics with naïve Bayes. In order to derive trustworthy points, real-time and adaptive techniques for P-QRS-T waves identification and delineation have been studied and used. In addition, 7 features representing different intervals for the ECG signal were extracted and were used to label any heartbeat as normal or irregular as an input into the naive Bayes. In every previous identification or prediction method, the combination of these functions has never been used. The ESP was introduced using the latest 65-nm technology, covering 0.112 mm2 in total and with a total power consumption of 2.78 μW depending on the design constraints. Furthermore, the proposed ESP achieved excellent rhythmic prediction up to 3 hours before the start. On the out-of-sample validation results, prediction accuracy of 86 percent was achieved by ten times cross validation with a three-size window. Due to its limited area, low power and the high efficiency of the ESP, the chips for handheld, mobile devices can be embedded into a system.

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