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A NEW HEURISTIC APPROACH TO REDUCE STATIC POWER USING CLUSTERING ALGORITHM

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ABSTRACT:

Power Consumption of Very Large Scale Integrated (VLSI) Circuits has been rising at a terrifyingly precipitous rate. This proliferation in power consumption has made an influential concern in the pattern of CMOS VLSI circuits currently. The major sources of total power dissipation such as dynamic and static power are growing with every switch (ON/OFF) to smaller process geometries. Nevertheless, due to process scaling tendencies, static power has turn out to be a foremost factor of the total power dissipation in CMOS VLSI circuits. This paper mainly focuses to tackle the leakage problem in CMOS circuits using proposed heuristic approach with performance measures such as delay, power and area of any conventional CMOS circuit design. The circuit is implemented using Tanner Tool 15.1 in 250 nm CMOS technology and the result is compared with previous existing techniques.

Key words: *Leakage power, Low-power design, Power gating, Sleep transistor***.**

1. INTRODUCTION:

As the nanometer CMOS technology grows, the power dissipation has become an increasingly important factor in CMOS VLSI circuits [1]. More important in today's VLSI circuits and system design requires is reduction in power dissipation for a portable electronic devices. In most of the CMOS digital circuits, power dissipation consists of dynamic and static components [2]. In which dynamic power consumption occurs due to logic transitions causing logic gates to charge/discharge load capacitance. In order to reduce dynamic power consumption as well as to improve the circuit performance both the supply voltage and threshold voltage has been scaled down, which results increases in sub threshold leakage, thus it makes leakage power (static power) high. Hence, it becomes major factor in total power dissipation [3]. Many researchers have been undergone for the purpose of reducing static power in CMOS VLSI circuits. However, it shows better results in any one, either power or delay or performance. Overall, the main focus is to achieve better CMOS VLSI circuits with good in performance, less delay and area reduction for low-power, high-performance digital CMOS circuits. Thus, a new heuristic approach is proposed to reduce static power and providing a new universal way to design low power CMOS VLSI circuits.

2. REVIEW OF STATIC POWER:

An introduction of increasingly important effect of leakage in recent and upcoming technology is nothing but, the static or leakage power, which is consumed during the steady-state when no transitions occurs and it is the third component of total power dissipation in CMOS circuits as shown in equation [4],

$$P_{total} = P_{dynamic} + P_{short-circuit} \quad (1)$$

The sources of leakage such as Reverse Biased Diode Leakage (pn-junction leakage), sub threshold leakage, Gate Induced Drain Leakage (GIDL), Gate Oxide Tunneling and further hot-carrier effect and punch-through are identified and analyzed separately under PTV variations.

Reverse Biased Diode Leakage:

The reverse biased diode leakage(pn-junction leakage) is due to the parasitic diodes formed between the diffusion

region of the transistor and substrate, consumes power in the form of reverse bias current which is drawn from the power supply.

Sub-threshold Leakage:
Sub-threshold leakage or sub threshold drain current or sub-threshold conduction is the current that flows between the source and drain of a MOSFET when the transistor in sub threshold region i.e., for gate-to-source voltage below the threshold voltage.

Gate Induced Drain Leakage (GIDL):
Gate induced drain leakage (GIDL) current arises in the high electric field under the gate/drain overlap region causing deep depletion. GIDL occurs at low V_G and high V_D and generates carriers into the substrate and drain from surface traps or band-to-band tunneling.

Gate Oxide Tunneling:
Gate oxide tunneling current (I_{ox}) is present when the electric field at the gate is high enough to tunnel through the gate oxide layer. This phenomenon is common in scaled down devices with reduced oxide thickness.

3. EXISTING TECHNIQUES:

In this section, we briefly appraise existing leakage power reduction techniques. There are plentiful designs have been proposed in order to reduce standby leakage in CMOS VLSI circuits. Some of the existing design techniques are forced stack, sleepy keeper, sleepy stack etc [3, 4, 6, 8].In which forced stack approach is a new technique to reduce leakage (static) power is to stack the transistors. The impact of stacking the transistors results in the reduction of sub threshold leakage current when two or more transistors are turned off together. Thus the reduction in leakage current for larger circuits is typically in the range of 10% to 30%.The second one is sleepy stack technique which is the combination of both the sleep transistor approach (used in active mode) and stack approach (used in sleep mode). By the help of stack approach, the existing in the design is divided into two transistors each typically with same width $'W_1'$, half the size of the original single transistor's width $'W_2$. After that, sleep transistor are added in parallel to one of the transistors in each set of two stacked transistors. The divided transistors reduce leakage power using the stack effect even though retaining the exact logic state. The operation of the added sleep transistors are turned ON during active mode and turned OFF during sleep mode. Thereby the stacked transistors suppress the leakage current in the sleepy stack approach. Sleepy Keeper approach is a another neoteric technique to reduce the leakage power in the CMOS VLSI circuits. Normally, in CMOS inverter, PMOS transistor connects to V_{DD} and NMOS transistor connects to GND. This one is familiar to everyone, that PMOS transistors are not competent at passing GND. In the same way, those NMOS transistors are not competent at passing V_{DD}. In spite of this, to maintain a value '1' in sleep mode, assuming, value'1' has already been premeditated. Thus sleepy keeper approach uses this output value of '1' and NMOS transistor connected to V_{DD} to maintain output value equal to '1' when in sleep mode. An additional single NMOS transistor located in parallel to pull-up sleep transistor connects V_{DD} to pull-up network. When in idle mode this NMOS transistor is the only source of V_{DD} to pull-up network, since the sleep transistor is OFF. Similarly, the reverse operation of above mentioned is performed on pull-down network. Hence, the leakage current is minimized by turn OFF the sleep transistor during sleep mode. But, the major drawback of forced stack approach is that, the reduction in leakage current for larger circuits is typically only in the range of 10% to 30% [5] and conversely, the limitation of sleepy stack technique is increase in area, since every transistor is replaced by three transistors [7].

3. PROPOSED WORK:

In this section, the proposed work is briefly explained. In order to overcome the drawbacks of forced stack, sleepy stack, sleepy keeper techniques such as low leakage reduction, increases area and delay, a new algorithmic technique was introduced. The main focus is to reduce static (leakage) power in CMOS VLSI circuits with good performance measures such as delay, power and area. Thus, a conventional CMOS circuit is choosen and it is implemented with proposed ideas and the results will be compared with previous existing methods.

A.Conventional CMOS Design:
To exemplify our skill, a conventional CMOS design is choosen, namely 4:1 multiplexer (combinational circuit) and it is implemented in tanner tool using S-Edit along with circuit performances such as power is measured.

B.Clustering Algorithm:

The Clustering Algorithm involves two steps, namely Preprocessing and Clustering. They are as follows:

1.Preprocessing:

The major intention of the preprocessing stage is to grouping the gates into subclusters such that the combination should not beyond the maximum current of any gate with in the cluster. Arbitrarily, choosen input siganls are applied and highest discharging (leakage) current at the output of every gate is examined. The discharge current is only examined since this is the current that flows through the sleep transistor and finally ground. The possibility that discharging takes place (switching activity) at the output of each gate is calculated and multiplied by the corresponding discharge peak current. This current is self-possessed of the discharge and short-circuit currents that takes place during switching. The peak current value and time at which switching occursalong with its duration are examined. The time the switching takes place depends on the gate's propagation delay and input pattern at the same time as the current duration depends on the slope of the input signal in addition the fanout of the gate. The greater the input slope and/or gate fanout, the higher switching duration. The discharge current of each gate takes a triangular shape, whose peak occurs at a time equal to the gate delay and periods a time , mainly in the fanout of the gate [9].

2.Clustering:

After implementation of conventional CMOS design using tanner tool and find the highest discharging current at the output of every gate. Then perform clustering in the implementation where the maximum leakage current present. Heuristic for grouping gate is shown in Fig. 1.

```
                CLUSTERING HEURISTIC
Create_Clusters()
1. Perform Conventional CMOS design
2. Initialize maxgates_per_cluster=n;
3. Create clusters with Single gates;
4. For cl=2; cl ≤ maxgates_per_cluster
        Create_n_Gate_Cluster(cl)
5. For all cluster created calculate highest discharging
        current at the output of each clusters
Create_n_Gate_Clusters(cl)
    1.  For cluster of type cl
        Create_new_cluster()
        While not done
        Choose Gate with minimum distance
        If sum of currents ≤ capacity
          affix gate to newly created cluster
        If total gates within cluster ≥ limit
            break;
        End
    2.  return newly created cluster
```

Fig 1: Heuristic for Grouping Gates

C.Power Gating:

Power Gating is a technique used in IC design to reduce power consumption, by shutting OFF the currents to blocks of the circuit that are not in use and also it is an effective approach to minimize standby leakage even though keeping high speed in the active mode. Power gating is based on the principle of adding devices, called sleep transistors, in series to the pull-up and/or the pull-down of the logic gates, and turning them off when the circuit is idle, thereby decreasing the leakage component I_{DS} due to sub-threshold currents. Now, the sleep transistors are going to be inserted in the group of clusters of implementation where the maximum leakage current present.There by the leakage power has been reduced by turning them ON during standby mode (SLEEP =1) and turing them OFF (SLEEP = 0) during active mode.Thus reults more leakage savings with good performance. Conventional power gating architecture is shown in Fig.2 [10].

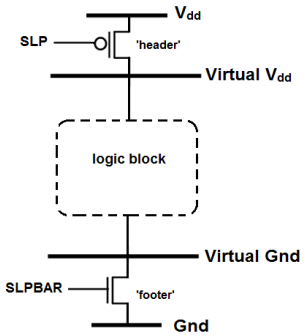

Fig 2: Conventional Power gating Architecture

4. SIMULATION AND RESULTS:

In order to implement the proposed ideas, a conventional CMOS design is performed and it is simulated with & without sleep approach as shown in Fig.3 & 4.

4:1 MUX Implementation:

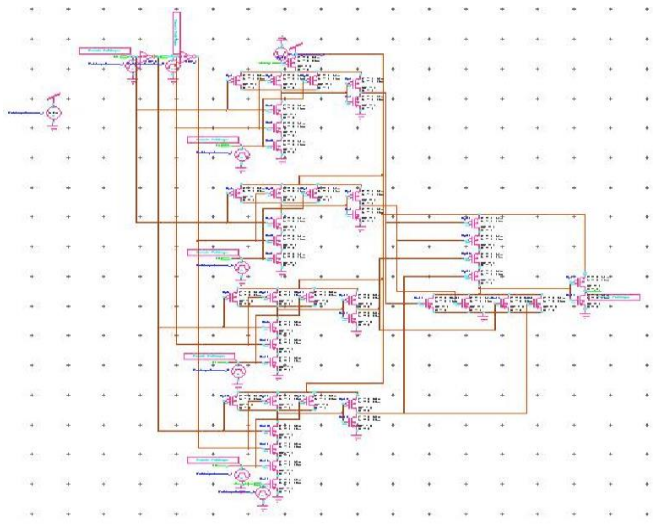

Fig 3:Transistor level implementation of 4:1 MUX using SLEEP Approach

Output Waveform:

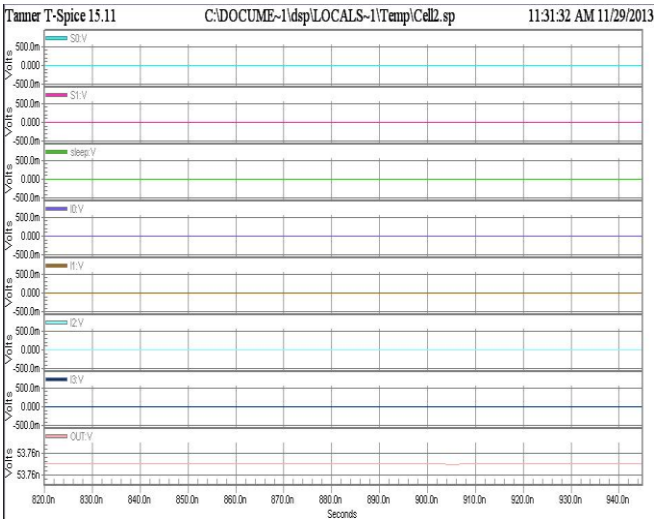

Fig 4: Output waveform of 4:1 MUX(standby mode)

Fig 4: Output waveform of 4:1 MUX(standby mode)

Performance Measures:

Parameter	With sleep transistor	Without sleep transistor
Leakage Power	2.842344e-017 watts	1.272648e-011 watts
Performance	Good	Poor

Table 1: Performance Measures of 4:1 MUX

5.CONCLUSION AND FUTURE WORK:

As technology scales down, it leads increase in leakage current and becomes a primary concern for low power, high-performance CMOS VLSI circuits. In this paper, an efficient algorithm is used in order to reduce static power and the proposed ideas are implemented in a Conventional CMOS design.Thus results, better leakage savings with reduction in power. Future Work involves, that the same proposed ideas will be implemented in any one of the conventional CMOS circuit and Clustering Algorithm is to be used in the same design. Thereby, expects more leakage savings with good circuit performance such as reduction in area, power and delay.

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