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DESIGN AND DEVELOPMENT OF APPROXIMATE MULTIPLIER USING REVERSIBLE LOGIC

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Abstract: **With evolving DSP applications, there is a need for faster and power efficient multiplier. Reversible logic is a promising field which addresses the problem of power dissipation. Vedic mathematics is the most efficient method for solving various problems. In this paper Vedic multiplier using Urdhva Triyakbhyam algorithm with Reversible logic is designed in Verilog HDL, simulated using Xilinx ISE 14.1 simulator and synthesized using Cadence EDA tool. In this work, delay and power consumption of n bit Vedic multiplier using basic Urdhva algorithm is compared with the Vedic multiplier using Reversible logic and the synthesize result shown that the Vedic multiplier with Reversible logic is more efficient. This multiplier can be used in different applications like convolution, cryptography, and communication etc., System performance is decided by the speed of the multiplier, that is the most important element in the numerous applications like Microprocessor, Digital signal processing. The implementation of Vedic multiplier using reversible gates improves the speed of operation and reduces power consumption.**

Keywords- **Vedic Multiplier, Urdhva Triyakbhyam, Reversible Logic, power, delay, Verilog HDL.**

I. INTRODUCTION

Vedic mathematics is the earliest Indian system of mathematics which offers the easiest way of calculations. Vedic mathematics can be applicable to numerous branches of mathematics. Vedic mathematics was reconstructed from the earliest Indian Vedas by Sri Bharathi Krishna Tirthaji after his study on Vedas. He created 16 different sutras. The famous among those sixteen sutras are Nikhilam Sutra, Urdhva Tiryakbhyam, and Anurupye. It has been found that Urdhva Tiryakbhyam is the maximum efficient among those.

Urdhva Tiryakbahayam algorithm is used in the application for all types for multiplication. The other name of Urdhva algorithm is “Vertical and Cross-wise” technique which enhance the speed of multiplication. This paper deals with the comparison of the various n bit Vedic multiplier mainly in terms of power and delay. From the survey it is find that the Reversible Vedic multiplier based on the Urdhva Triyakbhyam algorithm provides the best results in terms of delay and power. Reversible logic is one of the most promising fields for future low power design. Reversible logic gate provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

II. VEDIC MULTIPLIER

Vedic multiplier is the one which can be used for performing multiplication operation with the use of several algorithms. Urdhva Triyakbhyam (UT) is one of the 16 different sutras based on Vedic mathematical algorithms formulated by ancient Indian Vedic mathematicians. The “Urdhva Triyakbhyam” Sutra is the preferred multiplication formula relevant to all cases of multiplication along with binary, decimal and hexadecimal numbers. The Sanskrit name “Urdhva” means “Vertically” and “Triyakbhyam‟ means “crosswise”. Fig.1 shows an example of Urdhva Triyakbhyam. The partial product generation and the addition of the partial products are performed in a single stage of operation. Because of this parallel operation the speed of the multiplier is improved significantly when compared to other algorithms of Vedic mathematics. The Vedic multiplier is based on the Vedic multiplication algorithms. These algorithms are used for the multiplication of two decimal numbers. Here, we apply the same procedure to the binary numbers.

The Sanskrit name of vertically crosswise technique is ‘Urdhva Triyakbhyam’ which is a universal algorithm for multiplication. This method multiplies the digits vertically and crosswise and finally adds them using appropriate adder. This rule is applicable to both binary numbers and integers. The best feature of this method is that the partial products needed for the multiplication are already generated in advance and this leads to decrease in delay and power consumption. The increase in

number of bits however increases area and critical delay. Urdhva Triyakbhyam sutra is also called as vertically crosswise technique. The increase in area and delay with the increase in number of input bits is at slower rate when compared with other Vedic algorithms. Previously UT algorithm is used only for the multiplication of decimal numbers. Now UT algorithm can also be used for the multiplication of two binary numbers. Figure.3 explains the 4 bit binary Vedic multiplication.

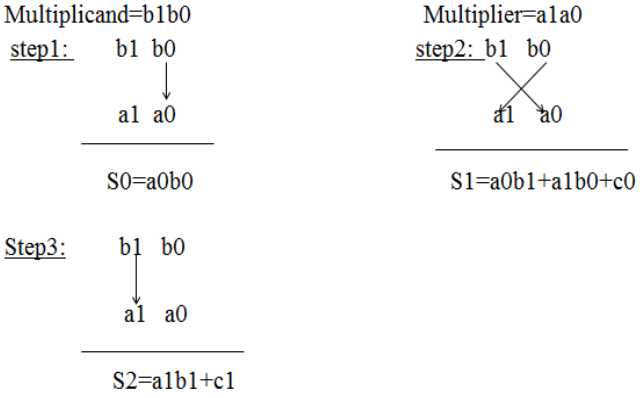

Fig.1 Urdhva Tiryakbhyam algorithm

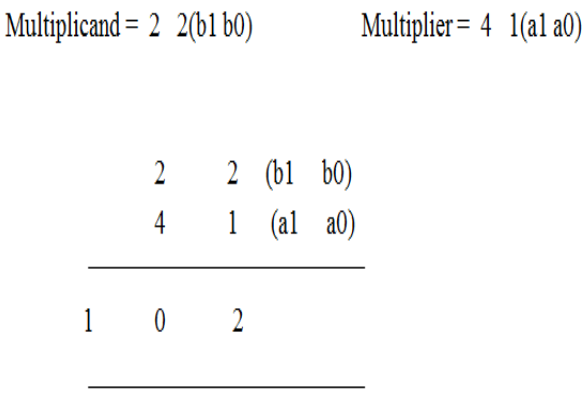

Fig.2 Example of 2bit Vedic multiplication using Urdhva algorithm

III. REVERSIBLE LOGIC

Reversible computing is the path to future computing technologies, which all happen to use reversible logic. In addition, reversible computing will become mandatory because of the necessity to decrease power consumption. Reversible logic circuits have the same number of inputs and outputs, and have one-to-one mapping between vectors of inputs and outputs, thus the vector of input states can be always reconstructed from the vector of output states. As with reversible gates, a reversible circuit has the same number of input and output wires, the reversible circuit with n inputs is called an n × n circuit, or a circuit on n wires.

A) Basic Reversible Logic Gates

1) Peres gate: Fig.3 shows the symbol of Peres gate. The inputs of the Peres gate are A,B,C and the outputs are P, Q, R The output is defined by P=A, Q=A^B, R=(AB)^C. The Quantum cost for this Peres gate is four.

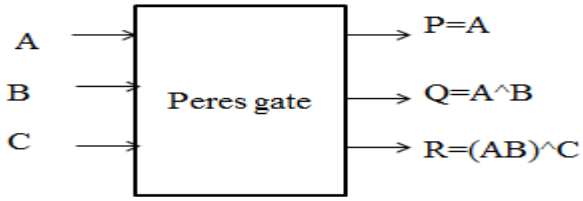

Fig.3 Peres gate

2) HNG gate: Fig.4 shows an HNG Gate. The inputs of an HNG gate are A, B, C, D and the outputs of the HNG gate are P=A, Q=B, R=(A^B)^C and S=((A^B)C)^(AB)^C. The combination of the Peres gate and HNG gate are used in the Ripple Carry Adder structure instead of using full adders. Therefore the delay can be reduced. The quantum cost for this HNG gate is six.

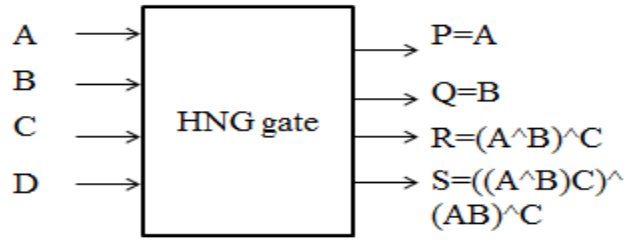

Fig.4 HNG gate

3) CNOT gate: Fig.5 shows symbol of CNOT gate. The inputs of the CNOT gate are X, Y and the outputs are X, X^Y. Since the part of the original input is obtained as output and due to reduced heat dissipation the information loss can be reduced using this Reversible logic. This is the main advantage of using this Reversible logic multiplier. The Quantum cost for the CNOT gate is one. The other name for this CNOT gate is Feynman gate.

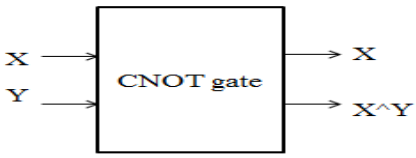

Fig.5 CNOT gate

The function f(x1, x2 … xn) of n Boolean variables is called reversible if:
1. The number of outputs is equal to the number of inputs.
2. Any input pattern maps to a unique output pattern.

B) Design parameters of Reversible logic gates:

1)Constant Inputs: The inputs that are necessary to perform a specific function which remain unaltered throughout the design.
2)Quantum cost: Quantum cost of a reversible circuit is that the overall quantum cost of all the logic gates used in it.
Quantum cost of a logic gate is decided by evaluating the number of primitive gates required to realize that reversible logic gate.
3)Gate count: Total number of reversible logic gates that are used to implement the logic circuit.
4)Garbage outputs: These are the outputs which are generated

due to the inputs but they are irrelevant to the required logic function. These outputs are vital to preserve the reversibility of the circuit but remains unused in the design.

5)Total Reversible Logic Implementation Cost (TRLIC): This refers to the summation of gate count, constant inputs, garbage outputs and quantum cost of the entire circuit.

IV. DESIGN METHODOLOGY

A) 2BIT VEDIC MULTIPLIER USING REVERSABLE LOGIC

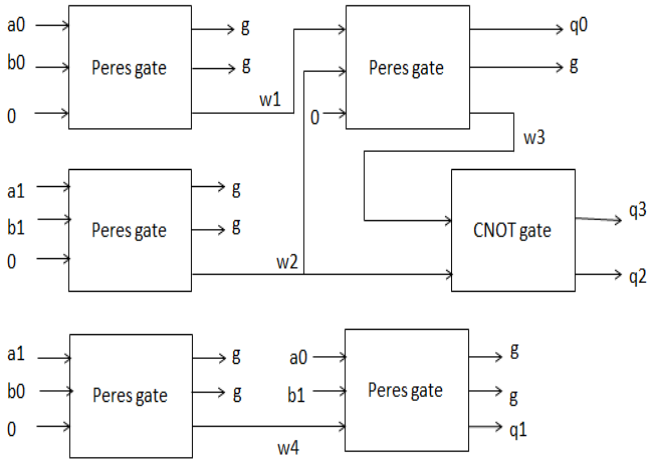

Fig.6 2bit Vedic multiplier using Reversible logic

The 2 bit Reversible multiplier using Reversible logic gates has two inputs as 2bit multiplier and 2bit multiplicand. The inputs are a[1:0] and b[1:0]. The implementation of Reversible logic multiplier for 2bit has 5 Peres gates and 1 CNOT gate. The Quantum cost for 2bit Reversible multiplier is 21 and the number of garbage output produced are 9. The implementation of 2bit Reversible multiplier requires 6 Reversible logic gates and 4 constant inputs. Therefore the TRLIC for this multiplier is 40. The block diagram for 2bit multiplier is shown in Fig.6.

B) 16BIT VEDIC MULTIPLIER USING REVERSIBLE LOGIC

The block diagram for 16bit multiplier is represented in Fig.7. In order to implement 16bit Vedic multiplier using Reversible logic, four 8bit Reversible logic multiplier has needed. The output from the Reversible multiplier is given to 16 bit Reversible adder. The input for 16 bit Vedic Reversible multiplier is represented as a[15:0] and b[15:0]. The result obtained is represented as s[31:0] and c3. The combination of Peres gate and CNOT gate is used to design Reversible multiplier and a chain of 16 HNG gates are used in designing Reversible adder. If the 16 bit Reversible adder using full adder block is replaced with a 16bit Carry Bypass adder using HNG gates, then the delay and the power consumption of the multiplier will be reduced and the comparison of delay and power is shown in Table.1 & Table.2.

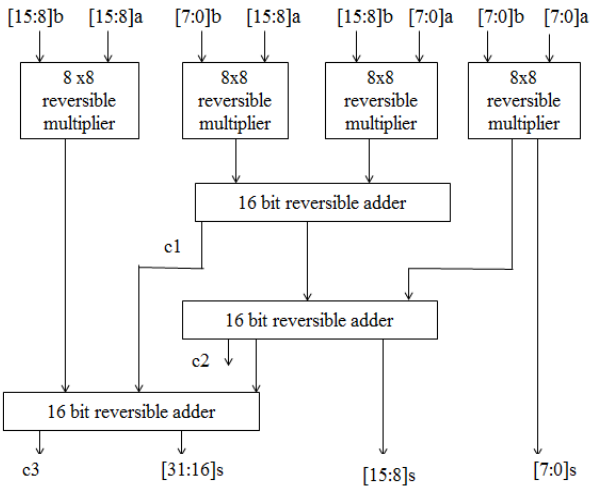

Fig.7 16bit Vedic multiplier using Reversible logic

C) 32BIT VEDIC MULTIPLIER USING REVERSIBLE LOGIC

To implement a 32 bit Vedic multiplier four 16bit Reversible multipliers and three 32 bit Reversible adders are needed. The output from the Reversible multiplier is given to three 32 bit Reversible adder. The inputs for 32 bit Vedic Reversible multiplier is represented as a[31:0] and b[31:0]. The result obtained is represented as s[63:0]and c3. . Then the 32 bit Reversible adder using full adder block is replaced with a 32bit Carry Bypass adder using HNG gates to reduce delay and power consumption. The 32bit Vedic multiplier is shown in Fig.8.

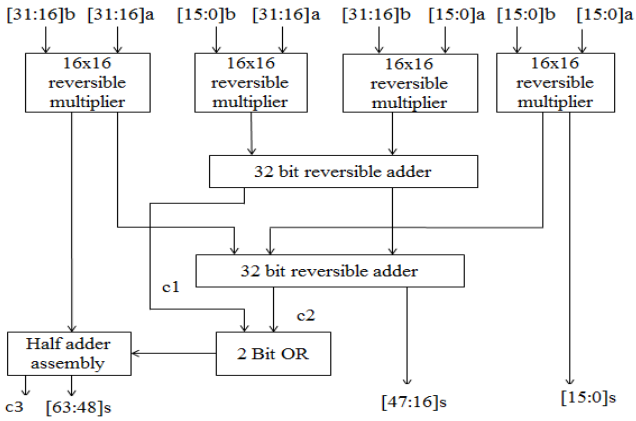

Fig.8 32bit Vedic multiplier using Reversible logic

D) 64BIT VEDIC MULTIPLIER USING REVERSIBLE LOGIC

Four 32bit Reversible multipliers and three 64 bit Reversible adders are used to implement a 64 bit Vedic multiplier. The input for 64 bit Vedic Reversible multiplier is represented as a[63:0] and b[63:0]. The result obtained is represented as s[127:0] and c3. . Then the 64 bit Reversible adder using full adder block is replaced with a 64bit Carry Bypass

adder. Since the operation of Carry Bypass adder depends on the propagate value the delay and power consumption can be reduced when any of the propagate value is 0. The block diagram for 64bit Vedic multiplier using Reversible logic is represented in Fig.9.

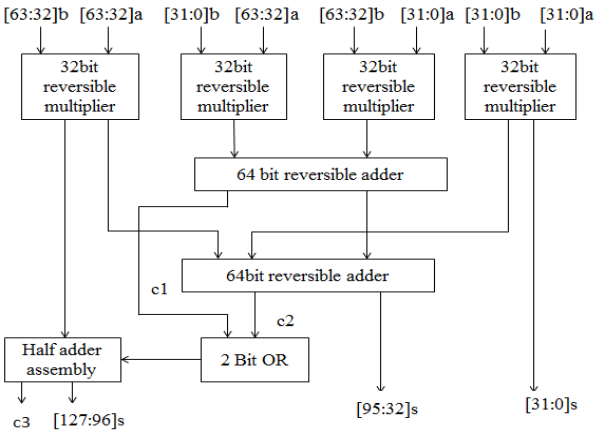

Fig.9 64bit Vedic multiplier using Reversible logic

E) 128BIT VEDIC MULTIPLIER USING REVERSIBLE LOGIC

The block diagram for 128bit multiplier is shown in Fig.10. The input for 128 bit Vedic Reversible multiplier is represented as a[127:0] and b[127:0]. The result obtained is represented as s[255:0] and c3. . The 128 bit Reversible adder using full adder block is used to obtain the sum and the carry bits. Then the Reversible adder is replaced with a 32bit Carry Bypass adder using HNG gates to reduce delay and power consumption.

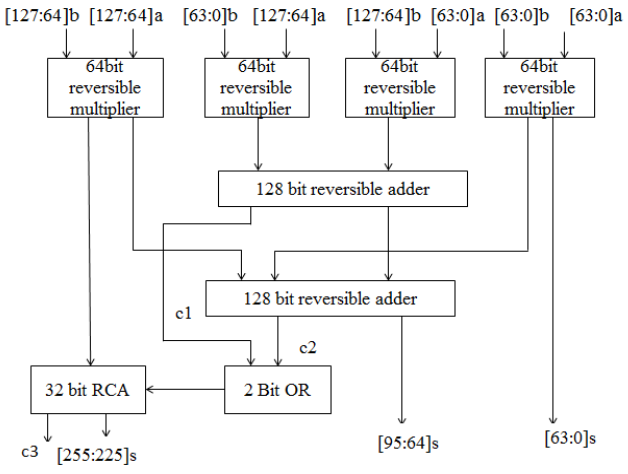

Fig.10 128bit Vedic multiplier using Reversible logic

V. PERFORMANCE ANALYSIS AND COMPARISON USING CADENCE EDA TOOL

A)DELAY COMPARISON USING CADENCE

Vedic multiplier using Reversible logic gates and Ripple carry adder using HNG gates is designed and synthesized using Cadence EDA tool and the ripple carry block is replaced with Carry Bypass adder in order to improve the speed of the multiplier. Then the delay comparison is shown in Table.1.

Table.1 Comparison of delay of n bit Vedic multipliers

PHASE 1 VEDIC MULTIPLIER	PHASE 2 REVERSIBLE MULTIPLIER WITH RIPPLE CARRY ADDER	MODIFIED REVERSIBLE MULTIPLIER WITH CARRY BYPASS ADDER
4bit: 2796 ps	4bit: 1365 ps	4bit: 1124 ps
8bit: 5866 ps	8bit: 5792 ps	8bit: 4556 ps
16bit: 11400 ps	16bit: 10145 ps	16bit: 7650 ps
32bit: 21660 ps	32bit: 17949 ps	32bit: 10337 ps
64bit: 42171 ps	64bit: 37672ps	64bit: 32672 ps

B) POWER COMPARISON USING CADENCE

The power value for n bit Vedic multipliers are obtained using Cadence and the values are compared. The comparison of power values obtained is shown in Table.2.

Table.2 Comparison of power of n bit Vedic multipliers

PHASE1 VEDIC MULTIPLIER USING UT ALGORITHM	PHASE 2 REVERSIBLE MULTIPLIER	MODIFIED REVERSIBLE MULTIPLIER USING CARRY BYPASS ADDER
4bit: 47767nw	4bit:47564nw	4bit: 48502nw
8bit: 344375nw	8bit: 329225nw	8bit: 314688nw
16bit: 2001151nw	16bit:1847306nw	16bit:1571815nw
32bit:10416921nw	32bit:9651467nw	32bit: 8071979nw
64bit:64904508nw	64bit:55453462nw	64bit:47904508nw

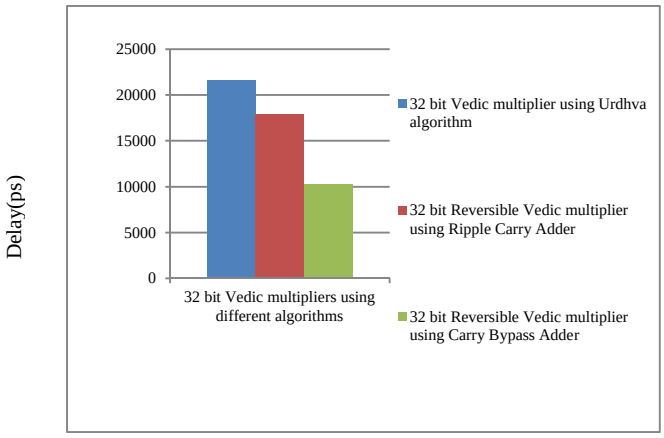

Fig.11 Comparison of delay for 32bit Vedic multiplier

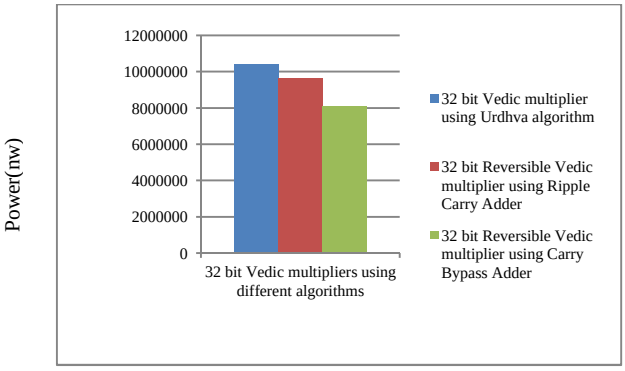

Fig.12 Comparison of power for 32bit Vedic multiplier

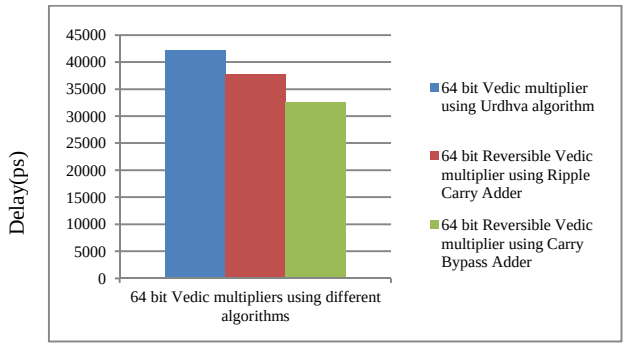

Fig.13 Comparison of delay for 64bit Vedic multiplier

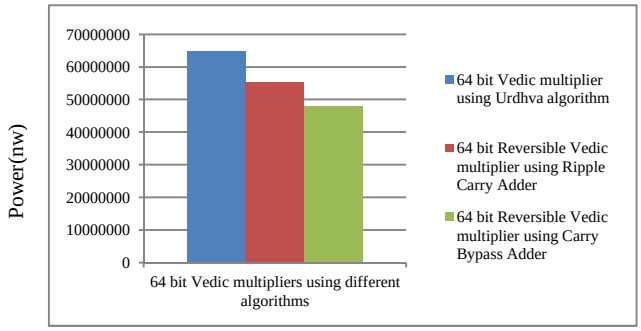

Fig.14 Comparison of power for 64bit Vedic multiplier

VI. SIMULATION RESULTS

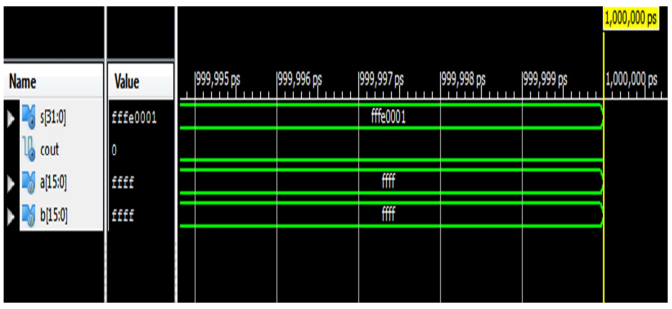

Fig.15 Simulation output for 16 bit Reversible Vedic multiplier

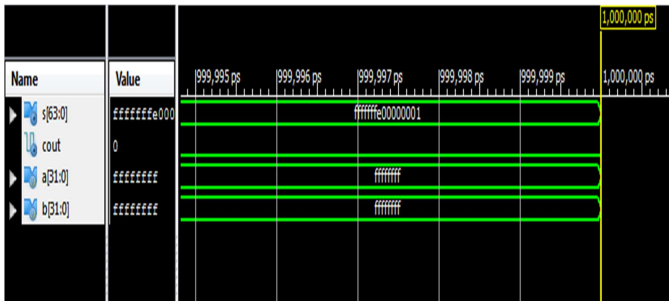

Fig.16 Simulation output for 32 bit Reversible Vedic multiplier

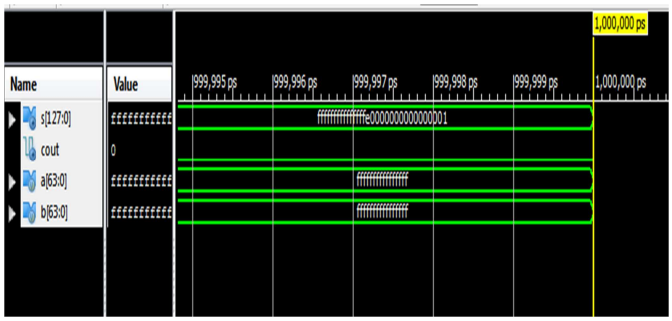

Fig.17 Simulation output for 64 bit Reversible Vedic multiplier

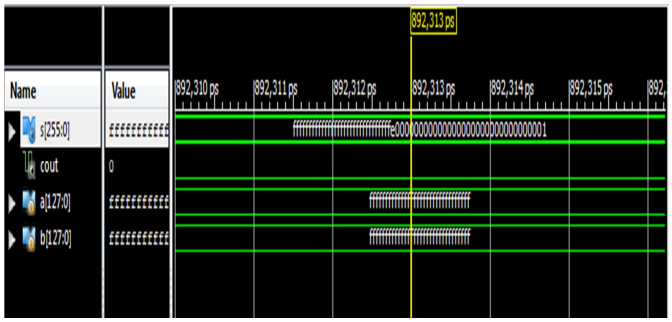

Fig.18 Simulation output for 128 bit Reversible Vedic multiplier

VII. CONCLUSION

In this paper the Vedic multiplier using reversible logic method for 128 bit have been discussed. As per study, the speed of the Vedic multiplier can be increased by using Reversible logic gates with Urdhva algorithm when compared with the conventional gates. This paper presents the performance of UrdhvaTriyakbhyam Vedic Multiplier using reversible logic gates. First 2bit UT multiplier is designed using Peres gate and Feynmen (CNOT) gate. The ripple carry adders used for the addition of partial products were constructed using HNG gates. If this ripple carry adder using Reversible logic gates are replaced with Carry Bypass adder then the maximum combinational path delay and power consumption can be reduced and the maximum combinational path delay obtained for 128 bit Vedic multiplier is obtained using Xilinx 14.1 simulator. The delay obtained for 128 bit Reversible multiplier is 246.37 ns.

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