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ANALAYSIS AND DESIGN OF CLOSED LOOP CASCADE VOLTAGE MULTIPLIER APPLIED TO TRANSFORMER LESS HIGH STEP UP DC-DC CONVERTER WITH PID CONTROLLER

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ABSTRACT
This paper proposes an analysis and design of closed loop cascade voltage multiplier applied to transformer less high step up dc-dc converter with PID controller. Providing constant output voltage, continuous input current with low ripple, high voltage ratio, and low voltage stress on the switches, diodes, and capacitors, the proposed converter is quite suitable for applying to low-input-level variable dc generation systems. Moreover, based on the *n*-stage Cockcroft–Walton (CW) voltage multiplier, the proposed converter can provide a suitable dc source for an (*n* + 1) level multilevel inverter.The simulation is carried over by the MATLAB/SIMULINK.

1. INTRODUCTION

In recent years, extensive use of electrical equipment has imposed severe demands for electrical energy, and this trend is constantly growing. Consequently, researchers and governments worldwide have made efforts on renewable energy. Applications for mitigating natural energy consumption and environmental concerns among various renewable energy sources, like wind energy, photovoltaic (PV) cell and fuel cell have been considered attractive choices.

However, without extra arrangements, the output voltages generated from the wind energy, photovoltaic (PV) cell are low level and variable. Thus, a high step up dc-dc converter is desired in the power conversion systems corresponding to these two energy sources. In addition to the mentioned applications, a high step-up dc-dc converter is also required by many industrial applications, such as high-intensity discharge lamp ballasts for automobile headlamps and battery backup systems for un interruptible power supplies.

Theoretically, the conventional boost dc-dc converter can provide a very high voltage gain by using an extremely high duty cycle. However, practically, parasitic elements associated with the inductor, capacitor, switch, and diode cannot be ignored,
and their effects reduce the theoretical voltage gain.

Up to now, many step-up dc-dc converters have been proposed to obtain high voltage ratios without extremely high duty cycle by using isolated transformers or coupled inductors.

Among these high step-up dc-dc converters, voltage-fed type sustains high input current ripple. Thus, providing low input current ripple and high voltage ratio, current-fed converters are generally superior to their counterparts.

In a traditional current-fed push–pull converter was presented to achieve high voltage gain, the leakage inductance of the transformer is relatively increased due to the high number of winding turns. Consequently, the switch is burdened with high voltage spikes across the switch at the turn-off instant. Thus, higher voltage-rating switches are required. Some modified current-fed converters integrated step-up transformers or coupled inductors, which focused on improving efficiency and reducing voltage stress, were presented to achieve high voltage gain without extremely high duty cycle.

Most of them are associated with soft switching or energy-regeneration techniques. However, the design of the high-frequency

transformers, coupled inductors, or resonant components for these converters is relatively complex compared with the conventional boost dc-dc converter.

1.1 ALTERNATIVE STEP UP DC-DC CONVERTER

Some other alternative step-up dc-dc converters without step-up transformers and coupled inductors are presented. By cascading diode–capacitor or diode-inductor modules, these kinds of dc-dc converters provide not only high voltage gain but also simple and robust structures. Moreover, the control methods for conventional dc-dc converters can easily adapt to them. However, for most of these cascaded structures, the voltage stress on each individual switch and passive element depends on the number of stages.

Figure 1.1 shows an *n*-stage cascade boost converter proposed for obtaining a high voltage gain. However, the passive elements and switch sustained high voltage stress in this cascaded converter.

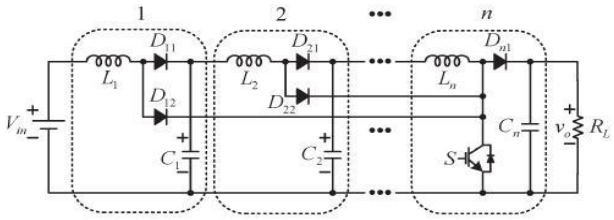


Fig 1.1 n-stage cascade boost converter

Figure 1.2 consists of a conventional boost converter and an n-stage diode–capacitor multiplier detailed. The main advantage of this topology is that higher voltage gain can easily be obtained by adding the stages of the diode-capacitor multipliers without modifying the main switch circuit. Nevertheless, the voltage across each capacitor in each switched capacitor stage goes higher when a higher stage converter is used.

Fig 1.2 Diode-capacitor *n*-stage step-up multiplier converter

Figure 1.3 shows another similar topology which has advantages similar to that of the previous topology. However, the voltage stress on the capacitors of higher stage is still rather high.

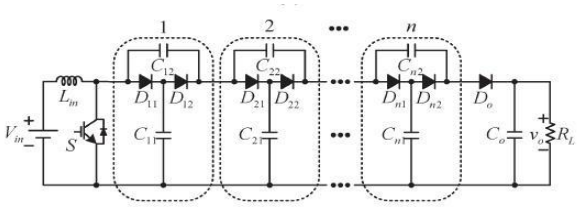


Fig 1.3 Boost converter with cascade voltage multiplier cells

2. PROPOSED CONVERTER

In this paper, a high step-up converter based on the CW voltage multiplier is proposed. Replacing the step-up transformer with the boost-type structure, the proposed converter provides higher voltage ratio than that of the conventional CW voltage multiplier. Thus, the proposed converter is suitable for power conversion applications where high voltage gains are desired. Moreover, the proposed converter operates in continuous conduction mode (CCM), so the switch stresses, switching losses and EMI noise can be reduced as well. The PID controller is used to get the constant output voltage whenever the input voltage changed.

Block diagram of proposed converter system:

Nevertheless, the proposed converter still demonstrates some special features:

1) In open loop four switches operate at two independent frequencies, which provide coordination between the output ripple and system efficiency.

2) With same voltage level, the number of semiconductors in the proposed Converter is competing with some cascaded dc-dc converters.

3) The dc output formed by series capacitors is suitable for powering multilevel inverters.

4) This system adopt for variable input DC source with the use of PID controller.

5) The proposed converter can adapt to an ac–dc converter with the same topology, and that will be a future work of this paper.

2.1 STEADY-STATE ANALYSIS OF

PROPOSED CONVERTER

$$S_D = \max\{x_k\} \quad \text{for} \begin{cases} i_\gamma > 0, k = 2, 4, \ldots, 2n \\ i_\gamma < 0, k = 1, 3, \ldots, 2n-1 \end{cases}$$

Figure 2.1 shows the proposed converter, which is supplied by a low-level dc source, such as

battery, PV module, or fuel cell sources. The proposed converter deploys four switches, in which Sc_1 and Sc_2 are used to generate an alternating source to feed into the CW voltage multiplier and Sm_1 and Sm_2 are used to control the inductor energy to obtain a boost performance. This will increase the complexity and cost of the proposed converter because an isolated circuit is necessary to drive the power semiconductor switches.

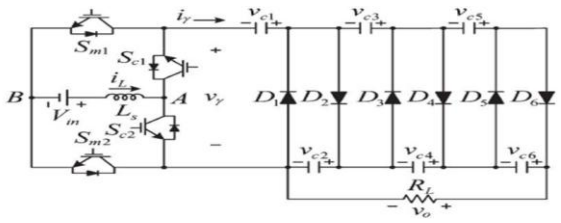


Fig 2.1 voltage- fed converter with cascade voltage multiplier

The proposed converter consists of one boost inductor Ls, four switches (Sm_1, Sm_2, Sc_1, and Sc_2) and one n-stage CW voltage multiplier. Sm_1 (Sc_1) and Sm_2 (Sc_2).Operate in complementary mode, and the operating frequencies of Sm_1 and Sc_1 are defined as fsm and fsc, respectively.

For convenience, fsm is denoted as modulation frequency, and fsc is denoted as alternating frequency. Theoretically, these two frequencies should be as high as possible so that smaller inductor and capacitors can be used in this circuit. In this paper, fsm is set much higher than fsc, and the output voltage is regulated by controlling the duty cycle of Sm_1 and Sm_2, while the output voltage ripple can be adjusted by fsc.

As shown in Fig. the well-known CW voltage multiplier is constructed by a cascade of stages with each stage containing two capacitors and two diodes. In an n-stage CW voltage multiplier, there are N (= 2n) capacitors and N diodes.

For convenience, both capacitors and diodes are divided into odd group and even group according to their suffixes, as denoted in Figure 2.1.

2.2 MATHAMETICAL MODEL

The concept of the negative voltage generation depicted in Fig 2.1. By connecting the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance *C*PV is clamped to zero. This prevents any leakage current flowing through it. With respect to the ground point N, the voltage at midpoint B is either zero or $+V_{dc}$, according to the state of the switch bridge. The purpose of introducing virtual DC bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one. As shown in Fig.4, the positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or $-V_{dc}$. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely $+V_{dc}$, zero and the CM current is eliminated naturally by the structure of the circuit, there's not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double frequency SPWM can be used to satisfy various PV applications.

$$\frac{diL}{dt} = \frac{1}{Ls}\left[vin - (dsc - dsm).v_{y}\right]$$

Where V_{in} is the input voltage, i_L is the input current, and the terminal voltage of the CW voltage multiplier. Assuming that the converter operates in CCM, the current the CW voltage multiplier depends on d_{sm} and d_{sc} expressed as where the current i_y can be deemed a pulse-form current source. In the mathematical model of a Cvoltage multiplier was discussed and simplified the equivalent circuit, which was convenient for simulation work.

Thus, according to the analyzing, the circuit behaviour of the load-side part (CW voltage multiplier) will be detailed in the following. For convenience, a current stage CW voltage multiplier energized by a sinusoidal ac source with line frequency, is used to analyze the steady behaviour of the CW circuit through simulation.

It can be seen from Fig.2.1 positive half cycle, that only one of the even diodes is conducted with the sequence *D*6, *D*4, and (odd) capacitors are charged (discharge conducting diodes. Similar behaviour occurs during the negative half cycle, while the odd diodes are conducted with the sequence *D*5, *D*3, and *D*1 and the odd (even) capacitors are charged (discharged).

Where S_D is an integer with values from 0 to 2 as diode-conducting index, for example, when represents that all diodes are not conducted and when represents that the diode *D*6 is conducted; {xk} is a set of diode conducting indices used to determine integer determined by i_y. When i_y = 0, either in positive or negative half cycles, we have k = 0 $x_{0=}0$ and {xk}=0, Thus, S_D

= 0 represents that all diodes are not conducted. When $i_y > 0$ in positive half cycle, We have =2,4,..2n and xk can be determined by,

$$x_k = \begin{cases} k, & \text{for } k \le 2 \\ k, & \text{for } k > 2 \text{ and } v_{c(k-1)} > v_{c(k)} \\ 0, & \text{for } k > 2 \text{ and } v_{c(k-1)} \le v_{c(k)} \end{cases}$$

In this paper, a high step-up dc-dc converter based on the CW voltage multiplier without a line- or high transformer has been presented to obtain a high voltage gain. Since the voltage stress on the active switches, diodes, and capacitors is not affected by the number of cascaded stages, power components with the same voltage ratings can be selected. The mathematical modelling, circuit operation, design considerations, and control strategy were discussed. The control strategy of the proposed converter can be easily implemented with a commercial average IC with adding a programmed CPLD.

The proposed control strategy employs two independent frequencies, one of which operates at high frequency to minimize the size of the inductor while the other one operates at relatively low frequency according to the desired output voltage ripple. Finally, the simulation and experimental results proved the validity of theoretical analysis and the feasibility of the proposed converter.

2.3 CIRCUIT OPERATION PRINCIPLE

State 1:

Sm_1 and Sc_1 are turned on, and Sm_2, Sc_2, and all CW diodes are turned off, as shown in Figure. The boost inductor is charged by the input dc source, the even group Capacitors C_6, C_4, and C_2 supply the load, and the odd-group capacitors C_5, C_3, and C_1 are floating.

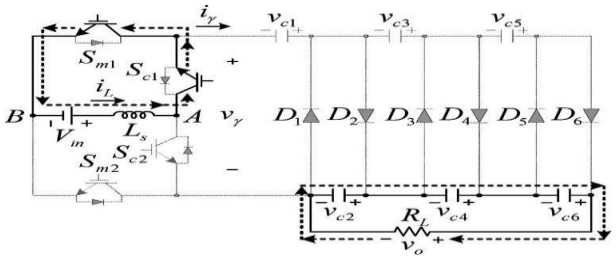


Fig 2.3 Conducting paths of three-stage CW voltage multiplier converter (State 1)

State 2:

Sm_2 and Sc_1 are turned on, Sm_1 and Sc_2 are turned off, and the current I_γ is positive. The boost inductor and input dc source transfer energy to the CW voltage multiplier through different even diodes.

State 2-A:

D_6 is conducting; thus, the even-group capacitors C_6, C_4, and C_2 are charged, and the odd-group capacitors C_5, C_3, and C_1 are discharged by Ia.

D_4 is conducting. Thus, C_4 and C_2 are charged, C_3 and C_1 are discharged by Ia C_6 supplies load current, and C_5 is floating.

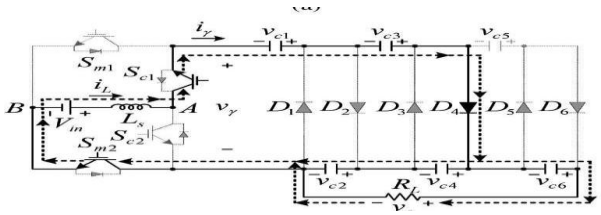


Fig 2.5 Conducting paths of three-stage CW voltage multiplier converter

State 2-C:

D_2 is conducting. Thus, C_2 is charged, C_1 is discharged by Ia, C_6 and C_4 supply load current, and C_5 and C_3 are floating.

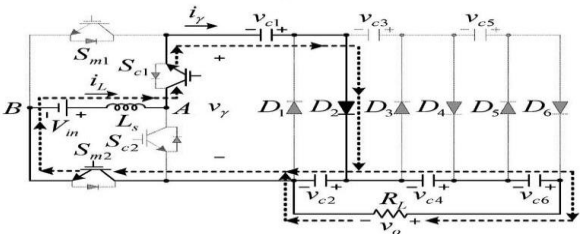
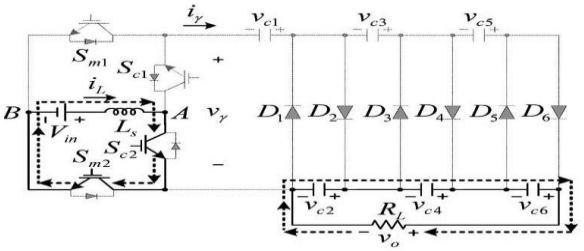


Fig 2.6 Conducting paths of three-stage CW voltage multiplier converter

State 3:

Sm_2 and Sc_2 are turned on, and Sm_1, Sc_1 and all CW diodes are turned off, as shown in Figure. The boost inductor is charged by the input dc source, the even group capacitors C_6, C_4, and C_2 supply the load, and the odd-group capacitors C_5, C_3, and C_1 are floating.



State 4:

Sm_1 and Sc_2 are turned on, Sm_2 and Sc_1 are turned off, and the current Iγ is negative. The boost inductor and input dc source transfer energy to the CW voltage multiplier through different odd diodes, as shown in figure 2.8

State 4-B:

D_3 is conducting. Thus, C_2 is discharged, C_3 and C_1 are charged by iγ, C_6 and C_4 supply load current, and C_5 is floating.

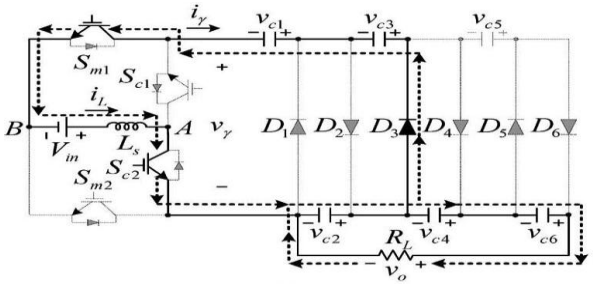


Fig 2.9 Conducting paths of three-stage CW voltage multiplier converter (State 4-B)

State 4-C:

D_1 is conducting. Thus, C_1 is charged by iγ, all even capacitors supply load current, and C_5 and C_3 are floating.

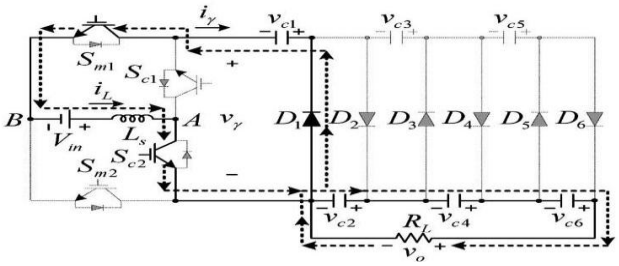


Fig 2.10 Conducting paths of three-stage CW voltage multiplier converter

(State 4-C)

2.3.1 IDEAL WAWEFORM OF PROPOSED CONVERTER

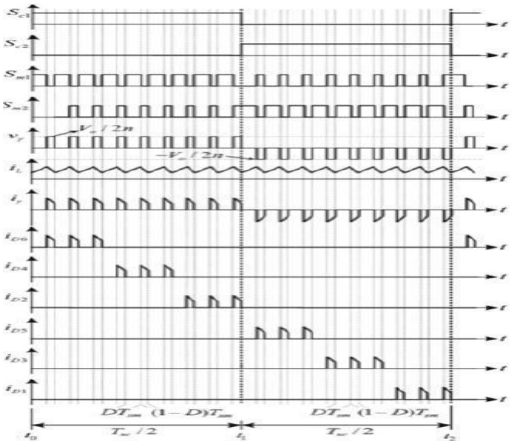


Fig 2.3.1 Ideal waveform of proposed converter

3. PID CONTROLLER

The PID controller is used for closed loop system. When the input voltage is varied the output voltage maintain constant. It calculates the error value from the output feedback (measured variable) with process value.

ERROR=Measured process variable-Desired set point

PID=Proportional + Integral + Derivative controller

For open loop transfer function,
U(s)/E(s) = KP+KdS+Ki/s
Kp= Proportional Gain
Kd= Derivative Gain
Ki= Integrative Gain
The gain value is measured by Ziegler Nichols method

4. SIMULATION RESULTS

The simulation circuit diagram of proposed converter is shown in Fig.3.

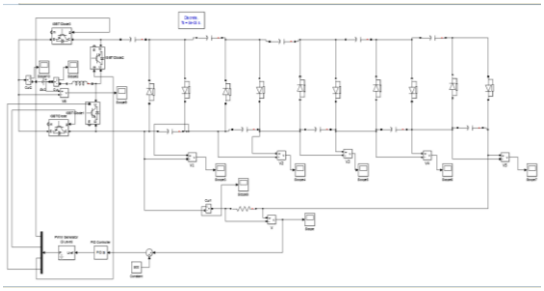
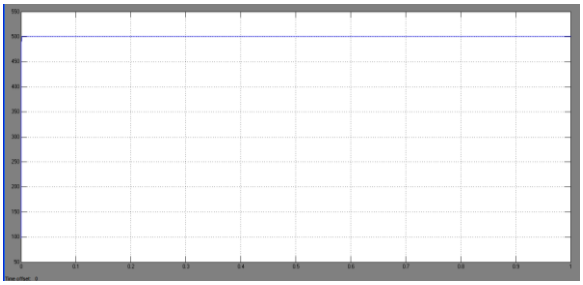
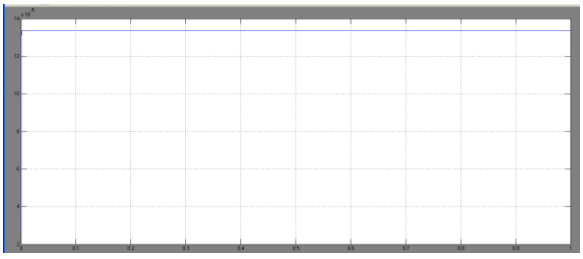


Fig.3 Simulation Model of Multi Port DC-DC Converter

Output voltage



Output current



5. CONCLUSION

In this paper, analysis and design of closed loop cascade voltage multiplier applied to transformer less high step up dc-dc converter with PID controller has been presented to obtain a high voltage gain and constant voltage. The voltage stress on the active switches, diodes, and capacitors are not affected by the number of cascaded stages, power components with the same voltage ratings can be selected. The proposed control strategy employs when the input voltage is variable to maintain constant voltage in output.

Finally, the simulation and experimental results proved the validity of theoretical analysis and the feasibility of the proposed converter.

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