

A CONTROL METHOD FOR VOLTAGE OSCILLATION SUPPRESSION USING NEUTRAL-POINT-CLAMPED INVERTER

P.Loganathan, K.Kamaraj

Assistant Professor, Department Of Eee, V.M.K.V Engineering College
Pg Scholar, Department Of Eee, V.M.K.V Engineering College

surya.jp07@gmail.com
kamarajdivya@gmail.com

Abstract— The major problem in the electrical power quality is the harmonic content. There are several methods indicating the quantity of harmonic content and the most widely used measure is the Total Harmonic Distortion. If total capacitance of DC-link capacitor is smaller, the amplitude of oscillation is larger. In this paper, three-level neutral-point-clamped inverter system is analyzed by the small-signal modeling and the control method reducing the oscillation of the neutral-point voltage is proposed. By the proposed method, the amplitude of the neutral point voltage oscillation is reduced. A nine level cascaded multilevel inverter power circuit is simulated in MATLAB simulink with sinusoidal PWM technique. The results are presented and analyzed.

Key words— NPC, Oscillation Suppression, Modulation Index, THD, Discontinuous pulse width modulation (DPWM), Low frequency oscillation, Neutral-point voltage balancing,

I. INTRODUCTION

The Pulse Width Modulated (PWM) inverters can control their output voltage and frequency simultaneously and also they can reduce the harmonic components in load currents. These features have made them suitable in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power conversion systems. The popular single-phase inverters adopt the full bridge type using approximate sinusoidal modulation technique as the power circuits. The output voltage of them has three values: zero, positive and negative of supply DC voltage levels. Therefore, the harmonic components of their output voltage are determined by the carrier frequency and switching functions [1]. However, three-level NPC inverter has a problem with the neutral-point voltage fluctuation inherently.

The neutral-point voltage should be controlled for good performance of the inverter system. To control the neutral-point voltage, the various control methods have been studied and introduced in many papers [5-10]. One of drawbacks that the conventional control methods have is a low frequency oscillation of the neutral point voltage. Some modulation methods have been proposed for improving this drawback. However, these methods have another drawback such as the complicated calculation processor the additional control loop.

To analyze the dynamic characteristic and control the performance of the inverter system to the various variations, the accurate model of the system is essential [11]. However, the detailed analysis of three-phase grid-connected three-level neutral-point-clamped (3P-GC-3L-NPC) inverter has not been done completely. The switching model and the switching function model predict the detailed transient response and the system behavior precisely [12], but these models are very complicated and need a long time to construct the models. Compared with switching model and switching function model, the averaged small-signal model is the more

simplified model due to approximation of the real switching model. The appropriate compromise between the accuracy to analyze and the complexity to construct model leads the widespread use of the averaged small-signal model. The averaged small-signal model is derived by averaging and perturbing and linearizing the circuit equations of the system. The derived model is used to design control system and to obtain the control-to-output transfer function and input-to-output transfer function.

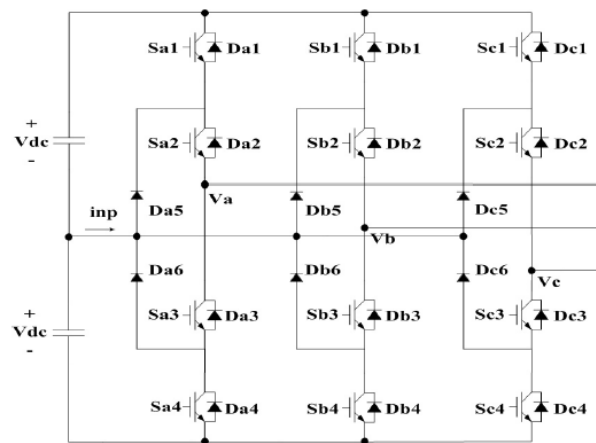


Figure. 1 Structure of three level inverter

3L-NPC inverter in Fig. 1 is a widely used topology of multi-level inverter. This NPC topology has inherent problem which is the neutral-point voltage caused by the neutral-point current that flows into or out from the neutral-point according to switching states. The unbalance and low frequency oscillation of the dc-link capacitor voltage cause the increase of the harmonic components and the destruction of the switching devices. Therefore, the analysis and the control of the neutral point current is very important issue. The maximum output phase voltage is given by $V_0 = V_1 + V_2 + V_3 + V_4$.

Each unit generates a quasi-square waveform by phase shifting its position and negative phase-leg-switching timings. It should be noted that each switching device always conducts for 180° (or half-cycle), regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching device current stresses equal. With enough levels and an appropriate switching algorithm, the multilevel inverter results in an output voltage that is near sinusoidal. The output voltage of the nine level cascaded multi-level inverter is shown in figure 2.

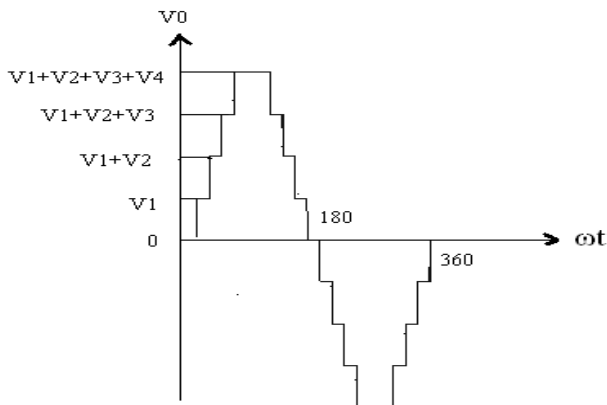


Figure .2 Output voltage of single phase cascaded nine level inverter

II. EXISTING METHOD

The conventional control method for two-level inverters is very simple and easily implemented. However, there are some drawbacks, such as high total harmonic distortion (THD) of the output waveforms, high voltage stress of the switching devices, low system efficiency. This is especially true in middle and high voltage, or high power conversions. Akira Nabae proposed a new neutral-point clamped (NPC) PWM inverter in 1980, which is the basic three-level inverter [1]. Comparing with the conventional two-level inverter, the three-level inverter has many advantages, such as low voltage stress on switching devices, high equivalent switching frequency, reduced output harmonics, etc.. Therefore, it is widely used in middle and high voltage, or high power applications [1], [4].

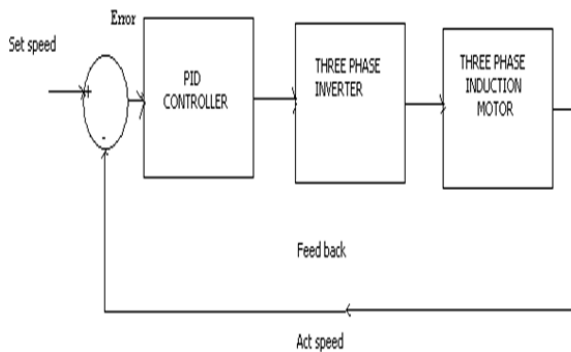


Figure.3. Block diagram of Existing Method

In order to generate phase voltage with three-levels and line voltage with five-levels, the NPC three-level inverter circuit needs two DC bus capacitors connected in series between the positive and negative poles of the DC bus. Ideally, the voltage on each capacitor is half the DC bus voltage. However, due to capacitance errors of the capacitors, different parameters of the switching devices, unbalanced three-phase operation, and other factors, a DC bus neutral-point voltage unbalancing problem appears, which influences the output waveforms quality [2], [6]. In addition, this problem makes the output waveforms contain a lot of low frequency harmonics. When the neutral-point voltage unbalancing problem becomes serious, it damages the switching devices and affects the system operation [6]. To solve this problem, many methods have been proposed. The neutral-point voltage unbalancing problem contains two parts: the dc deviation and the low frequency oscillation of the neutral-point voltage. The

dc deviation of the neutral-point voltage can be controlled by many solutions proposed in the literature.

For example, zero-sequence voltage injection methods have been proposed in [2], [7]. Ref. [3], [5] propose improved space vector modulation (SVM) methods to reduce the neutral-point voltage unbalancing. In addition, they correctly select other vectors, which do not impact on the neutral-point voltage, to replace the small vectors. The low frequency oscillation of the neutral-point voltage can lead to a lot of low frequency harmonics in the output waveforms, and the voltage stress of the switches is increased [4], [10]-[11]. When the dc deviation of the neutral-point voltage appears, the low frequency oscillation problem can also exacerbate the neutral-point voltage unbalancing, especially in middle or high power applications.

However, the low-frequency oscillation problem of the neutral-point voltage is commonly ignored. A new modulation strategy using small vectors to compensate for the effects of all of the vectors in each carrier cycle is proposed to reduce the neutral-point voltage ripple. Ref. [4] proposes a double modulation wave strategy based on SPWM to enable the average neutral-point current to be zero. So the low frequency oscillation of the neutral-point voltage is eliminated. However, it has a much higher switching frequency when compared with the conventional SPWM control method. Based on the basic principle of discontinuous pulse width modulation (DPWM), this paper proposes a new DPWM control method to suppress the low frequency oscillation of the neutral-point voltage. By distinguishing the odd and even carrier cycles, and the prior and latter half carrier cycles, the proposed method controls the switches of a certain phase so that there is no switching in each carrier cycle.

In addition, in each carrier cycle, the operating time of the positive and negative small vectors in pairs is equal. Therefore, the average value of the neutral-point current is zero in a carrier cycle, and a neutral-point voltage without low frequency oscillation can be achieved. When compared with the conventional SPWM control, without adding complex hardware circuits or increasing the switching frequency, the new DPWM control method proposed in this paper can suppress the low frequency oscillation of the neutral-point voltage effectively under different load conditions. This decreases the output waveforms harmonics and significantly increases the system efficiency. The proposed DPWM control method is easy to achieve with digital implementation. Experiments have been realized by a NPC three-level inverter

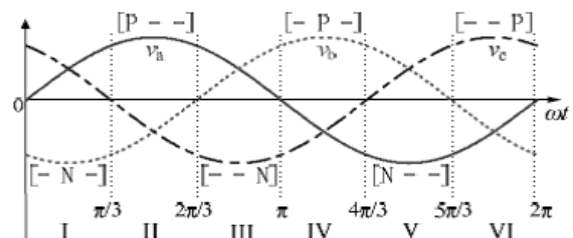


Fig. 2. The operating principle of 60 DPWM.

The regions are defined as follows: (0- $\pi/3$), II($\pi/3-2\pi/3$), III($2\pi/3-\pi$), IV($\pi-4\pi/3$), V($4\pi/3-5\pi/3$), and VI($5\pi/3-2\pi$). In each region, the switches of one certain phase keep no switching. So the corresponding output level is in the "P" or "N" state, the details are as follows:

(1) In regions I (0- $\pi/3$), III ($2\pi/3-\pi$), and V ($4\pi/3-5\pi/3$), for the phase modulation wave with the lowest voltage value, the corresponding switches S_{x3} , S_{x4} of this phase are kept in the

on-state, and the switches Sx1, Sx2 of this phase are kept in the off-state. Therefore, the output phase leg is in the “N” state, (2) In regions II($\pi/3-2\pi/3$), IV($\pi-4\pi/3$), and VI($5\pi/3-2\pi$), for the phase modulation wave with the highest voltage value, the corresponding switches Sx1, Sx2 of this phase are kept in the on-state, and the switches Sx3, Sx4 of this phase are kept in the off-state. Therefore, the output phase leg is in the “P” state.

III. PROPOSED METHOD

The power electronic equipment such as inverter have switching devices and their operation produces current and voltage harmonics into the system from which they are working. These harmonics affect the operation of their equipments connected to the same system through the injection of harmonics. The even order harmonics are eliminated by using filters. The odd order harmonics can be eliminated by various techniques. The analysis of the harmonics and harmonic reduction by PWM techniques are described in this section.

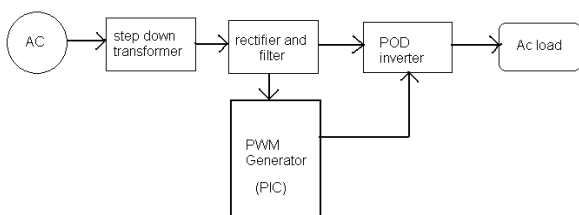


Figure.3. Block diagram of Proposed Method

The performance of each of these PWM control methods are based on the following parameters: a) Total harmonic distortion (THD) of the voltage and current at the output of the inverter, b) Switching losses within the inverter, c) Peak-to-peak ripple in the load current, and d) Maximum inverter output voltage for a given DC rail voltage. Thus the choice of a particular PWM technique depends upon the permissible harmonic content in the inverter output voltage. From above mentioned PWM control methods are applied in the proposed inverter since it has various advantages over other techniques. Sinusoidal PWM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage [6]. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. Sinusoidal pulse width modulation is one of the primitive techniques, which is used to suppress harmonics presented in the quasi-square wave. In the modulation techniques, there is an important parameter i.e., the ratio $M = A_r/A_c$ known as modulation index, where A_r is reference signal amplitude and A_c is carrier signal amplitude.

The HESA is assumed to be the quarter-wave symmetric. Fourier series of the quarter-wave symmetric S H-bridge cell multilevel inverter output waveform is written as follows

$$V(\omega t) = \sum_{n=1}^{\infty} \frac{4V_{dc}}{n\pi} \left[\sum_{k=1}^s \cos(n\theta_k) \right] \sin(n\omega t) \quad (1)$$

Where the optimized switching angles, which must satisfy the following condition

$$\theta_1 < \theta_2 < \dots < \theta_s < \pi/2 \quad (2)$$

The amplitude of all odd harmonic components including fundamental one, are given by

$$h(n) = \frac{4V_{dc}}{n\pi} \sum_{k=1}^s \cos(n\theta_k) \quad (3)$$

The switching angles of the waveform will be adjusted to get the lowest output voltage THD. If need to control the peak value

of the output voltage to be V_1 and eliminate the third and fifth order harmonics, modulation index is given by

$$M = \frac{\pi V_1}{4V_{dc}} \quad (4)$$

The resulting harmonic equations are

$$\frac{4V_{dc}}{\pi} [\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)] = V_1 \quad (5)$$

$$[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4)] = 0 \quad (6)$$

$$[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4)] = 0 \quad (7)$$

$$[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)] = M \quad (8)$$

To determine the switching angles for Selective Harmonic Eliminated PWM (SHEPWM) cascaded multilevel inverter. Such switching angles are defined by a set of nonlinear equations to be solved. In the case of two possible solutions for an angle θ_i , the criteria for selecting one of them can be the Total Harmonic Distortion (THD). The best angle values are therefore the ones leading to the lowest THD.

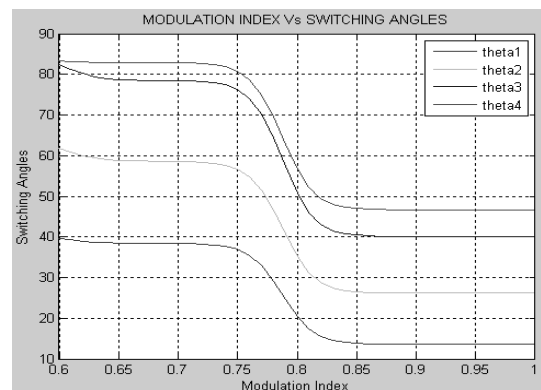


Fig. 3 Plot for Modulation index Vs corresponding Switching Angles

In the case of two possible solutions for an angle θ_i , the criteria for selecting one of them can be the Total Harmonic Distortion (THD). The best angle values are therefore the ones leading to the lowest THD. The number of inputs and outputs depends from the considered process. In our application, the feed forward neural network has to map the underlying relationship between the modulation rate (i/p) and the switching angles (o/p) as shown in figure 3. The figure 4 shows that the relationship between modulation rate and its calculated THD for their corresponding switching angle. In view to confirm the validity of obtained results using the harmonics elimination technique with neural network, a test is carried out for $M=0.8$. The switching angles for test data are obtained from the neural network such as its output (switching angle). From that switching angles, the desired level of carrier signal levels are obtained. The triangular carrier signal is compared with sinusoidal reference which results the triggering pulses for various switches. These pulses are used to trigger the nine level cascaded multilevel inverter. The output voltage and current waveform and its harmonics spectrum are shown in figure 7,8. *Advantages:* Number of switching device low compared to previous system. Due to POD modulation the output accuracy of converter and system power factor of the converter are to be maintained within the permissible limit. Our proposed converter produces a better performance on electric traction drive.

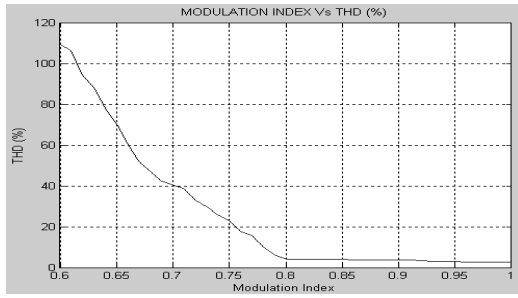


Fig. 4 Plot for Modulation index Vs THD in percentage

IV. SIMULATION RESULTS

The simulink model of the proposed nine level cascaded multilevel inverter systems for SPWM techniques with open loop, closed loop PI and neural implementation are described by following simulation diagrams. The simulation was done for a cascaded nine level inverter with sinusoidal pulse width modulation is described in following figures 7. The gating signals generated using sinusoidal PWM technique is given to the power circuit switches to obtain the output voltage. The Figure.5 shows the simulated output voltage and current

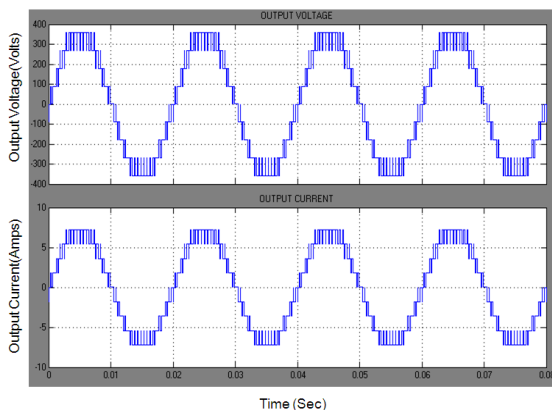


Fig. 5 Simulated output voltage and current waveform for sine PWM

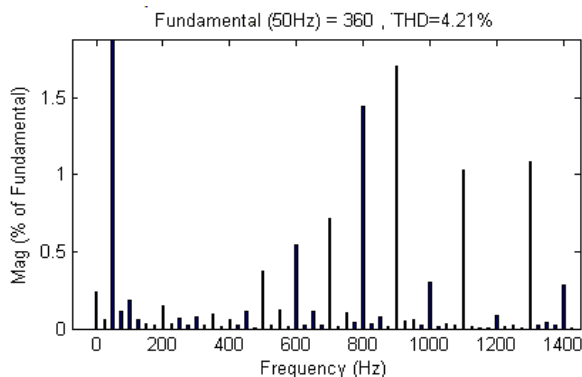


Fig. 6 Frequency spectrum of the output Voltage.

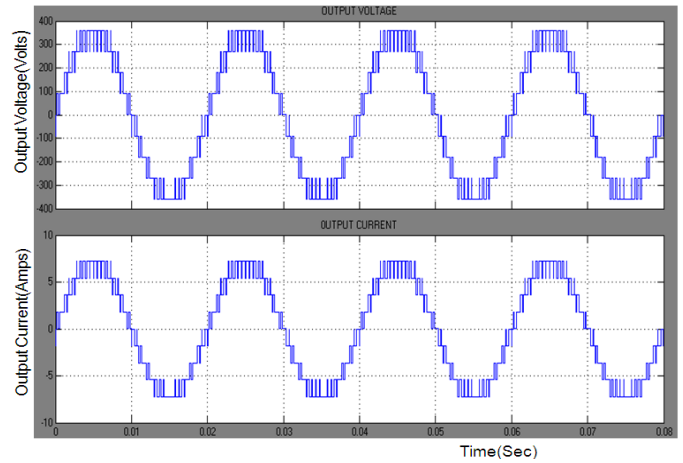


Fig. 7 Simulated output voltage and current waveform for sine PWM with Neural Network

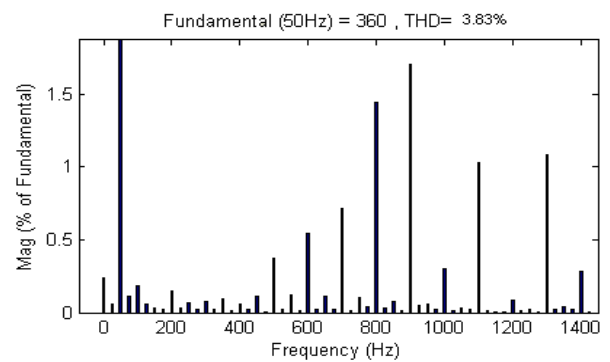


Fig. 8 Frequency Spectrum of the output voltage in Sine PWM with Neural Network

V. CONCLUSION

This paper has presented the three-level NPC inverter system and proposed the neutral-point voltage oscillation reduction method. The neutral-point current control by the small-signal modeling, the control-terms which are related to the neutral-point current control is set to zero for the reduction of the neutral-point voltage oscillation caused by the output phase current. The results show that the oscillation of the neutral-point voltage is reduced by the proposed method.

REFERENCES

- [1] MEENAKSHI, J. ; SREEDEVI, V.T, "Simulation of a transistor clamped H-bridge multilevel inverter and its comparison with a conventional H-bridge multilevel inverter" IEEE International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2014 , 20-21 March 2014
- [2] Kumar, D.V.A. ; Babu, C.S. "New multilevel inverter topology with reduced number of switches using advanced modulation strategies" IEEE International Conference on Power, Energy and Control (ICPEC), 2013 pages 693 – 699.
- [3] Haiwen Liu, Leon M. Tolbert, SurinKhomfoi, BurakOzpineci, Zhong Du, "Hybrid Cascaded Multilevel Inverter with PWM control Method", conference and proceedings , pp: 162-166 , June 2008.
- [4] P.C. Loh, D.G. Holmes, T.A. Lipo, "Implementation and control of distributed PWM cascaded multilevel inverter with minimum harmonic distortion and common mode voltages", IEEE Transactions on Power Electronics, vol. 20, no. 1, pp. 90-99, Jan. 2005.

- [5] Chiasson, J.N.; Tolbert, L.M.; McKenzie, K.J.; ZhongDu, "A Unified approach to solving the harmonic Elimination Equation in multilevel converters", IEEE Transactions On Power Electronics, Vol. pp: 478 – 490, March 2004
- [6] B. P. McGrath and D. G. Holmes, "Multicarrier PWM Strategies for multilevel inverters," IEEE Trans. Ind. Electron. vol. 49, no. 4, pp. 858–867, Aug. 2002.
- [7] Leon M. Tolbert, Senior member, IEEE, Fang ZhengPeng, Senior Member, IEEE, and Thomas G. Habetler, Senior Member, IEEE, " Multilevel PWM methods at Low modulation Indices" , IEEE Transactions On power Electronics, Vol. 15, No. 4, July 2000.
- [8] L.M.Tolbert and T.G.Habetler, "Novel Multilevel Inverter Carrier Based PWM methods", Proc.IEEE trans. Ind Applications, Vol.35, pp. 1098-1107, Sept.1999.
- [9] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," IEEE Trans. Power Electron., vol. 7, pp. 497–505, July 1992.
- [10] N.S. Choi, J. G. Cho, and G.H. Cho, "A general circuit topology of multilevel inverter," in Proc. IEEE PESC'91, pp. 96-103.
- [11] C. K. Duffey, R. P. Stratford, "Update of harmonic standard IEEE-519, IEEE recommended practices and requirement for harmonic control in electric power systems," IEEE Transactions on Industry Applications, vol. 25, no. 6, pp.1025-1034, Nov./Dec. 1989.
- [12] S. Wolfram, Mathematica, a System for Doing Mathematics by Computer, 2nd ed. Reading MA: Addison-Wesley, 1992.
- [13] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor converters: Part I-harmonic elimination," IEEE Trans. on Ind. Appl., Vol. 9, pp. 310-317, May/June 1973.
- [14] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor converters: Part II-voltage control technique," IEEE Trans. on Ind. Appl., Vol. 10, pp. 666-673, Sept./Oct. 1974.
- [15] N. Mohan, T. M. Undeland and W. P. Robbins, 2003 -Power Electronics: Converters , Applications, and Design, 3rd Edition. J. Wiley and Sons.
- [16] Khomfoi, S., Tolbert, L. M., "Fault Diagnostic System for a Multilevel Inverter Using a Neural Network", in IEEE Transactions on Power Electronics, Vol. 22, No. 3, pp. 1062-1069, May 2007.