International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)
ISSN: 0976-1353 Volume 29 Issue 6 – JULY 2022.

TEST PATTERN GENERATION WITH FAULT DETECTION

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***Abstract*— Through comparing such work to MISR, it is possible to identify the flaw that develops in electrical circuits. Through the compression of many bit streams into a single signature, the output response analyzer MISR speeds up the testing process. The creation of the bit streams utilizing pseudo-random pattern generators is the crucial component in this situation (PRPG). It has the anticipated output and is made up of a phase shifter and ROM. The MISR is then put to the test. The output is either the same as anticipated or different, depending on the answer given. A circuit is not defective if the expected output matches the actual output, otherwise. By using seemingly random patterns, faults might be found in this way..**

***Index Terms*— Multiple Input Signature Register (MISR), Pseudo-Random Pattern Generation (PRPG), Read Only Memory (ROM), Phase shifter, Fault detection.**

I. Introduction

TPG (Test Pattern Generator) input sequence allows automatic test methods to discern between the proper circuit behavior and the incorrect circuit behavior carried on by faults. The created patterns are applied to post-manufacture testing of semiconductor technology or to help identify failure mechanisms (Anudeep et al. (2022)). The basic goal of production trials will largely stay the same to assure high-quality, dependable moderately products conditions and as a result, test techniques may significantly change. The design process, design parameters, and semi-conductor technologies are some of the major aspects that will affect its progression. In order to deliver the appropriate test quality for the upcoming technological nodes, such three-dimensional, new sorts of faults will need to be taken into account. The major goal of the test pattern research is to identify circuit defects quickly and with little power consumption (Shivakumar et al. (2021)).

We suggest a PRPG for LP applications in this study. The generator's main goal is to lessen switching activity. It is capable of taking on a number of configurations that enable a specific scan chain to be powered either by a PRPG itself or by a constant value fixed for a certain amount of time. The Multiple Input Signature Register is another idea we have (MISR). An output response analyzer called MISR speeds up the testing process by condensing several bit streams into a single signature. The intended output is recorded in the ROM, and the MISR and ROM output are then contrasted using a comparator to look for any circuit faults.

II. RELATED WORKS

Shivakumar et al. (2021) suggested LFSR will produce effective pseudo-random test patterns that will be used in BIST designs. The suggested LFSR met the primary strategies, such as re-seeding and decreased test power usage, for the BIST designs. However, the optimum pseudo-random test patterns used the reseeding strategy. Warade and Ravi (2022)) proposed the use of Model Predictive Control (MPC) within BIST for the goal of reducing testing to guarantee that the system's power consumption and space usage are reduced. Low power (LP) testing pattern generator outcomes are contrasted with those of the model predictive control scheme for test compressor. When compared to built-in self-tests, this is advantageous for creating pseudo-random testing patterns, preferable toggling levels, and a superior gradient of fault coverage (BIST). This results in a binary representation with PRESTO activity, or preselected toggling. Mohammad et al. (2022) suggested test compression approach produces high-quality tests. Using the suggested technique, the 8-bit arithmetic logic unit (ALU) is evaluated, Power use and space utilization are highlighted. Chen et al. (2021) focused on attack timings are around one tenth of those of cutting-edge SAT-based attacks on the same defenses, and they recover keys up to 500 bits long in less than 7 seconds. Next, they show how our attacks may be expanded to scan chains that have been compressed using multiple input signature registers (MISRs). Suriyan et al. (2022) introduces specialized built-in self-test (BIST) method for scan-based circuits that might aid in energy conservation. Thanks to a mapping logic that modifies the LFSR's state transitions; only the accessible vectors are generated in a fixed series. As a result, the execution time of trials has dropped without affecting blame coverage. Circuit experiment shown that the linear feedback shift register significantly reduces power consumption during random testing.

III. PROPOSED WORK

Memory Chip Schematic Register Transfer Language (RTL) is the term. It displays the circuit's execution logic, including how input enters and exits the network. Due to the application of low power and RTL execution, we proposed a pseudo-random pattern generation for implementing low power application.

In hardware description languages (HDLs) like Verilog

and VHDL, register-transfer-level (RTL) is used to generate high-level descriptions of circuits from which lower-level representations and eventually literal routing may be obtained. Modern digital design is frequently done at the RTL level. During the circuit design stage of the electronic circuit design cycle, RTL is utilized. A circuit design tool often converts an RTL description of the design to a gate-level description of the circuit. After that, positioning and routed tools are employed to generate a physical layout using the findings of the synthesis. The RTL description of a design can be used by logic tools to evaluate its accuracy.

RTL schematic output is depicted as follows.

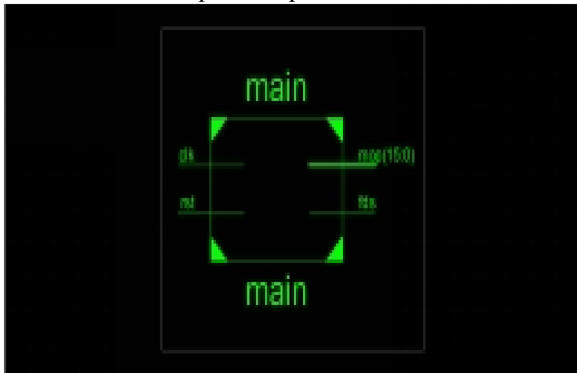

Figure 1: Main RTL schematic

Here, the clock and reset are the two inputs, then mop is the main output which is a 16 bit test pattern and fds is the output which gives the fault present in the circuit.

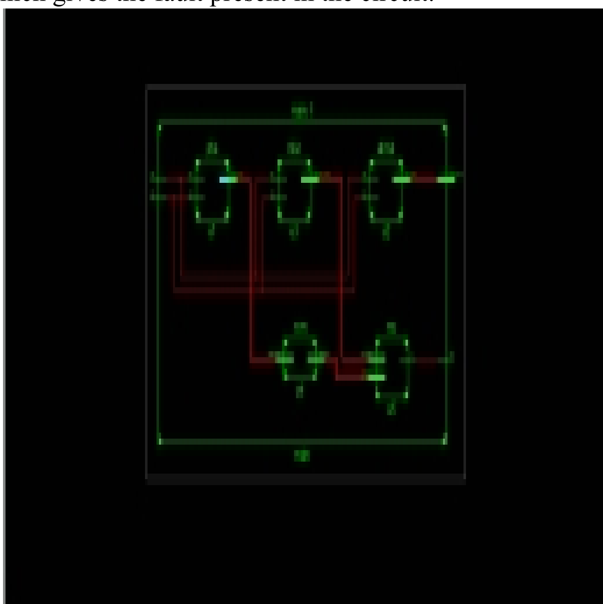

Figure 2: Entire RTL schematic model

It consists of

Phase Shifter

ROM

MISR

Multiplier Unit

Comparator

A. PHASE SHIFTER

In order to make particular sound wavelengths in or out of phase with one another, phase shifting involves taking the input signal; add a very slight delay to it, and then combining it back with the original signal. Since the time duration is regulated, the amount of delay varies with time.

Phase shift merely denotes that the two signals are, at any fixed instant, at various positions in transmission cycle. Phase shift, which depicts how each wave moves through its cycle, is calculated as the inclination (in degrees or radians) across given angles on a circle simultaneously moment. In devices like phase enhancers, bandwidth rise, scientific equipment, multi spectral antennas, etc., a phase shifter is employed.

B. READ ONLY MEMORY (ROM)

Computer storage chips that carry permanently or quasi data are referred to the memory that can only read from. During manufacturing, the data is constantly saved in such memory. Such start-up instructions for computers are kept in ROMs.

C. MULTIPLE INPUT SIGNATURE REGISTER (MISR)

As a substitute for n-parallel LFSRs, MISR is frequently utilized as a predicted optimal detector.

D. MULTIPLIER UNIT

Every bit of the multiplier's sub - blocks is calculated in concurrently when using a complementary multiplier.

A binary multiplier is an electrical circuit that multiplies two discrete integers in semiconductor technology, such as computers. A digital multiplier can be implemented using a variety of computer arithmetic methods.

E. COMPARATOR

Basically by comparing different inputs, the comparator circuit determines whether the output should be large ("1") or weak ("0").

IV. RESULTS AND DISCUSSION

Pseudo-random pattern generators of the TPG method appear to be a desirable alternative. Integrated circuits with several incoming and outgoing lines and relatively low resource - based use can be used as an example. The size of several input and output line chips, at least for a section of these circuits, determines how much space is used up substantially on a substrate material. This is the basis, a sizeable portion of the chip regions left available for an IC's internal logic are repetitive and can be utilized for the LBIST structure's requirements.

Figure 3: Output wave form for proposed method

Since it is preferable to optimize the run time with minimal limitations on size, standby time, and weight dedicated to batteries, it is crucial to reduce the overall power consumption in such systems. Therefore, low power design should be the primary consideration while creating processors for portable devices. Efficiency, budget, and power losses are the three key areas where VLSI has difficulties. Low power dissipation VLSI circuits are necessary for the implementations.

Figure 4: Power analysis of proposed work

V. CONCLUSION

The LP generator, PRESTO, is capable of producing pseudo-random test patterns with switching activity that is carefully chosen by autonomous coding, as demonstrated in the study. When compared to the fundamental design of a PreSelected Toggling (PRESTO) generator, fault coverage is provided with minimal power by using a comparator, Read Only Memory (ROM), and Multiple Input Signature Register (MISR). Where both methods can give high-quality testing by combining their strengths. As a result, it is a very appealing LP test technique that offers highly adjustable trade-offs between pattern counts and fault coverage. With a low power consumption of 0.06 watts, the XILINX ISE offers strong interactive capabilities for creating pseudo-random patterns and temporal limitations.

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