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Survey of Multi Level Integrated AC-DC Converter Control of DC Motor Applications

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Abstract— In this project a new integrated multi level AC-DC converter is proposed. The proposed converter has two independent controllers. First controller is used to control the input side and the second for the output side. The input controller prevents DC bus voltage from becoming excessive and performs power factor correction and regulates DC bus voltage. The output controller regulates output voltage for the variable load conditions. By adopting this system we can use it as a "DC DRIVER" for varying mechanical loads.

I. INTRODUCTION

The metric system of units has undergone a number of changes in its history, of which the latest is the SI (Systeme International d'Unites). This system has become popular in most of the industrialized world, largely because it is a coherent system, in which the product or quotient of two or more units is the unit of the resulting quantity. Certain simplifications result from using this form of the metric system.

In the Sl system, force IS measured in Newtons (N) and distance in meters (m). Consequently, the units of torque are Nm (see Table 1.). If a motor shaft rotates at an angular velocity of ωM radians per second, with torque TM, the mechanical power output will be equal to the product TM, and ωM and the units will be watts if TM is in Nm.

Motor manufacturers usually specify a torque constant (KT) and a voltage constant (KV) for their motors. These constants have different values when the torque and speed are measured in English units, but they have the same numerical value when Sl units are used. This becomes obvious when you consider that the electrical input power must be equal to the mechanical output power:

$$V_A I_A = T_A \omega_M \text{ (Watts)}$$

$$\frac{V_A}{\omega_M} = \frac{T_M}{I_A} = K_{TV}$$

Where VA is the internally generated armature voltage, or back emf and IA IS the armature current. (See Figure 1–1 for definition of motor terms.)

Table 1. Units Conversion

THESE UNITS	$\{\times \leftarrow = \rightarrow \div\}$	SI UNITS	DIM
oz	2.78×10^{-1}	N	MLT^{-2}
lb	4.448	N	MLT^{-2}
in	2.54×10^{-2}	m	L
ft	3.048×10^{-1}	m	L
gf	9.807×10^{-3}	N	MLT^{-2}
g cm^2	10^{-7}	Nm sec^2	ML^2
ft lb sec^2	1.356	Nm sec^2	ML^2
oz in sec^2	7.063×10^{-3}	Nm sec^2	ML^2
ft lb	1.356	Nm	ML^2T^{-2}
oz in	7.063×10^{-3}	Nm	ML^2T^{-2}

NOTE: The dimensions are M (mass), L (length), and T (time). The gram (g) is a unit of mass and the gram-force (gf) is a unit of force. The pound (lb) and the ounce (oz) are included as units of force only.

Applying the same principle to the familiar electrical transformer yields the turn's ratio:

Figure 1 show this series RLC circuit is an excellent model of a dc motor loaded with an essentially inertial load. Here, J is the total moment of inertia, including the rotor's JM.

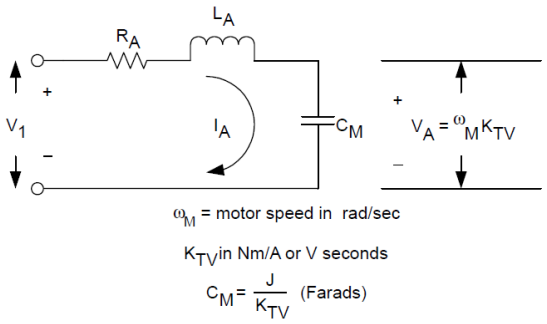


Figure 1. RLC Circuit

Thus, the non-dimensional turns ratio N1/N2 is analogous to the dimensional torque (or voltage) constant KTV. Furthermore, equations (2) and (4) give us a clear hint that the angular velocity (ωM) is analogous to voltage, while the torque (TM) is analogous to current.

The units of Km may be either Nm/A. or Vsec/rad. Thus, specifying both KT and KV for a motor is like measuring and specifying both the voltage ratio and the current ratio of a transformer, and can only make sense where redundancy is required.

II. Literature Review

[3] J. Marcos Alonso, Member, IEEE, Author Describe

The integrated buck-flyback converter (IBFC) has previously been proposed for other applications such as DC–DC conversion and electronic ballasts, but has not been well investigated for HPF off-line dc power supplies. When operated in DCM, since the ratio of the bulk capacitor voltage and the peak line voltage depends only on the buck and flyback inductance ratio, the use of the buck converter as ICS permits the operation with low bulk capacitor voltage. Thus, the conduction angle of the buck converter within the line half period is constant and Independent of the peak line voltage. On the other hand, a fast output regulation can be achieved with a proper design of the error amplifier, thus compensating the voltage ripple across the bulk capacitor, and limiting its value to the hold-up time requirement.

Another advantage of the IBFC that will be highlighted in this paper is that as opposed to other SS integrated converters, the control switch handles a considerably lower rms current. As will be shown, the current through the control switch is the buck or the flyback inductor current, whichever is higher, but not the addition of the two currents, as it occurs in other integrated converters. The remaining current is handled by the diodes of the integrated switch, which give lower losses due to their voltage-source equivalent behavior. This characteristic provides quite a higher efficiency for this type of DCM operated converters.

[21] Wu Chen, Student Member, IEEE, and Xinbo Ruan, Senior Member, IEEE Zero-Voltage-Switching PWM Hybrid Full-Bridge Three-Level Converter With Secondary-Voltage Clamping Scheme IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 55, NO. 2, FEBRUARY 2008

Although zero-voltage-switching (ZVS) is achieved for all the switches of the H-FB TL converter, with the use of the resonant inductance (including the leakage inductance of the transformer) and the intrinsic capacitors of the switches, there is voltage oscillation across the rectifier diodes caused by the reverse recovery, which should be damped by a lossy snubber.

An H-FB TL LLC resonant converter was proposed, and the rectifier diodes can achieve a zero-current-switching however, the stresses of the power semiconductors and the resonant components are increased remarkably. In order to eliminate the voltage oscillation across the rectifier diodes in ZVS FB and ZVS half-bridge (HB) TL converters, two clamping diodes are introduced to the primary side, and there are two arrangements for the positions of the resonant inductance and the transformer. It is better for the transformer to be connected with the lagging leg and the lagging switches in the FB and HB TL converters, respectively. Applying the aforementioned method to the H-FB TL converter, this paper introduces two clamping diodes to the primary side of the H-FB TL converter. They form a secondary-voltage clamping scheme, together with the resonant inductance and the transformer, to clamp the secondary rectified voltage at the reflected input voltage in the 3L mode and at the reflected half input voltage in the 2L mode, respectively. Thus, the oscillation across the rectifier diodes is eliminated, and the reverse-recovery loss can be alleviated.

[1] Jun-Young Lee, Student Member, IEEE Single-Stage AC/DC Converter With Input-Current Dead-Zone Control for Wide Input Voltage Ranges IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 54, NO. 2, APRIL 2007

The first one is the variable switching control method, but it has problems such as low conversion efficiency and/or difficulty in the optimal design of the filter and inductor. Other possible approaches are using magnetic feedback, and Parallel power processing. They can be applicable to converters with wide input-voltage ranges but still show high voltage stress and/or complex circuit structure.

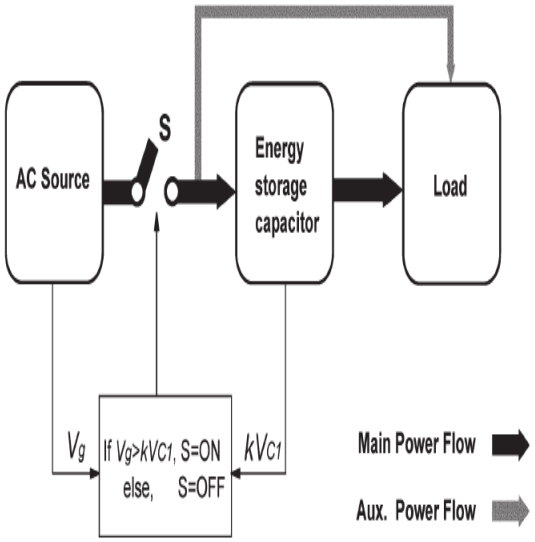
In this paper, an improved single-stage ac/dc converter is proposed to meet universal input requirements by using input-current dead zone control. It is derived from a basic DCM

flyback converter with two transformers. One of the transformers is used to control an amount of link capacitor charge current in such a way that the input-current dead zone becomes expanded according to the link voltage increase and shrunk in the opposite case. The proposed converter is tested with a 60-W (5-V 12-A output) prototype circuit. Experimental results show that the link voltage and switch stresses are lower than 384 and 500 V, respectively, at the 265-Vrms line voltage with 10% load.

III. Operational Principles

The proposed converter is depicted in Fig. 1. It is derived from a flyback converter whose two transformers are connected in series input and parallel output. The upper transformer T1 is used for delivering energy stored in the dc link capacitor C1 to the output. The lower transformer T2 delivers the input energy directly to the output, as well as dc-link energy, and has an additional function to limit the current charging into the link capacitor by controlling the input-current dead zone.

Accordingly, the proposed converter shows different operations depending on the input-current flow that is influenced by the voltage applied to the anode of D2. Fig. 2 depicts a powerflow diagram of the proposed converter. The power flow is controlled by the imaginary switch S, which is on or off based on the relationship between the rectified line voltage Vg and the link voltage VC1 scaled by k. k is a constant value between 0 and 1 that is determined by the primary inductances of the two transformers. If Vg is greater than kVC1, the switch S is on, and the input power is supplied to the link capacitor and output stage. In the opposite case, power transmission from the ac line is stopped, and the output power is supplied only by the link capacitor. Because the decision of the switching point of S varies according to the link capacitor voltage level, the charge current of the link capacitor can be further reduced as the link capacitor voltage is increased. It follows that an excessive



increase of the link voltage can be suppressed. Fig. shows the simplified diagram of the proposed converter when the main switch Q is turned on. Assuming that the anode voltage of D2 is lower than the cathode voltage, D2 is blocked, and the anode voltage ofD2 can be written as follows by applying Kirchhoff's voltage law (KVL) along C1, L2, and L3:

$$V_3 = \frac{L_3}{L_2 + L_3} V_{C1}$$

where L2 and L3 are primary inductances of T1 and T2, respectively. Therefore, the critical rectified line voltage Vg,critical that determines the diode state is defined as

$$V_{g,\text{critical}} = \frac{L_3}{L_2 + L_3} V_{C1}.$$

Introducing N, the inductance ratio of L2 to L3, (2) can be rewritten as

$$V_{g,\text{critical}} = \frac{1}{N+1} V_{C1}.$$

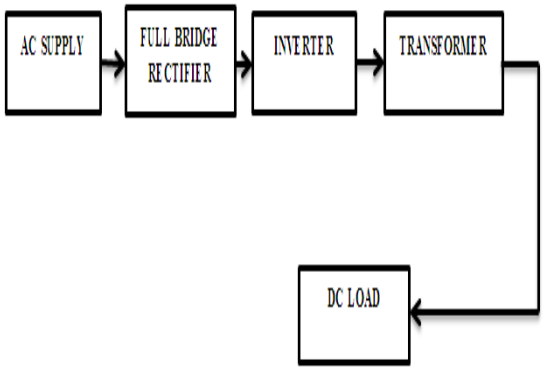
DCM condition is successfully satisfied by selecting the inductance ratio of L2 to L3. Because the main switch carries input inductor current as well as load current, the current stress is heavy in general. Accordingly, it is important to choose a proper value to make the current stress as low as possible. Referring to this, the maximum current stress can be written as follows:

$$I_{Q,\max} = \frac{V_3}{L_3} D_{\max} T_s$$

Where V3 is calculated from (10) with the peak value of the minimum line voltage. Fig. 8 shows the maximum current stress according to calculated (L1,N) pairs satisfying DCM, which shows that lower current stress can be obtained by selecting N to be as small as possible. Therefore, the (L1,N) = (43 μH, 1.6) pair is used for the design, and the power factor is predicted to be about 0.95 from (3), (4), and Fig. shows the reset time plots of ID3 and ID4 divided by (1 − Dmax)Ts according to the transformer turns ratios of n1 and n2 from (23) and (24). In this figure, the minimum transformer turns ratios of T1 and T2 are found to be 7.8 and 7.4, respectively, and n1 = 8 and n2 = 8 are used in the prototype converter. With these design parameters, the calculated maximum link voltage is about 395 V, and the maximum switch voltage stress is calculated as 475 V. The key component parameters used in the prototype.

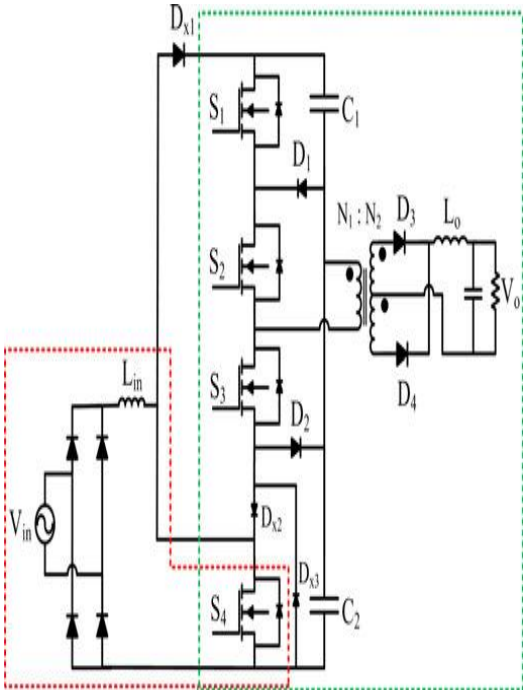
IV. Experimental Results

Three-level AC–DC converter is proposed. The proposed converter integrates the operation of the boost power factor correction and the three-level AC–DC Converter. There is only a single stage power factor correction converter; it is operated with two independent controllers. One controller is used to perform PFC and regulate the voltage across the primary side DC-bus capacitors. The other controller is used to regulate the output voltage, by sending appropriate gating signals.



Fig, integrates an AC–DC boost PFC converter into a three-level DC–DC converter. The AC–DC boost section consists of an input diode bridge, boost inductor Lin, boost diode Dx1, and switch S4, which is shared by the multilevel DC–DC section.

When S4 is off, it means that no more energy can be captured by the boost inductor. In this case, diode Dx2 prevents input current from flowing to the midpoint of capacitors C1 and C2 and diode Dx1



Conducts and helps to transfer the energy stored in the boost inductor Lin to the DC bus capacitor. Diode Dx3 bypasses Dx2 and makes a path for circulating current.

Although there is only a single converter, it is operated with two independent controllers. One controller is used to perform PFC and regulate the voltage across the primary side DC-bus capacitors by sending appropriate gating signals to S4. The other controller is used to regulate the output voltage by sending appropriate gating signals to S1 to S4. It should be noted that the control of the input section is decoupled from the control of the DC–DC section and thus can be designed separately. The gating signal of S1, however, is dependent on that of S4, which is the output of the input controller; how this signal is generated is discussed in detail later in this project.

The gating signals for S2 and S3 are easier to generate as both switches are each ON for half a switching cycle, but are never ON at the same time. Typical converter waveforms are shown in Fig

1) Reduced cost compared to two-stage converters: Although the proposed converter may seem expensive, the reality is that it can be cheaper than a conventional two-stage converter. This is because replacing a switch and its associated gate drive circuitry with four diodes reduces cost considerably even though the component count seems to be increased this is especially true if the diodes are ordered in bulk numbers.

2) Better performance than a single-stage converter: The proposed single-stage converter can operate with a better input power factor for universal input line applications than a single-controller, single-stage because it does have a dedicated controller for its input section that can perform PFC and regulate the DC-bus voltage. The presence of a second controller also allows the converter to operate with better efficiency and with less output ripple as each section of the converter can be made to operate in an optimal manner.

3) Improved light-load efficiency: The proposed converter can be designed so that it has a conventional DC-bus voltage of 400 V. Since the converter is a multilevel converter, a 400 V DC bus means that each switch will be exposed to a maximum voltage of 200 V. Having 200 V across a MOSFET device instead of 400 V (as is the case with two-level converters) results in a 75% reduction in turn on losses when the converter is operating under light-load conditions and there is an insufficient amount to current available to discharge the switch output capacitances before the switches are turned on. 4) Increased design flexibility: Since the converter is a multilevel converter, it can be operated with high dc-bus voltage (800 V), standard dc-bus voltage (400 V), or any dc-bus voltage 400 V < Vbus <800 V. There are advantages to operating with high dc-bus voltage or with standard dcbus voltage. The fact there is flexibility in the level that the dc-bus voltage is set means that there is considerable flexibility in the design of the converter.

V. Future Implementation

Through this analysis of such an input side regulate the DC-bus voltage and boost power factor correction. The output side is output voltage can be regulated. It was done by simulations. In future, i will use this for DC driver application in place of resistive load and gives the better implementation. As further step, and simulation result can be compared with the results obtained in practical set of conditions.

VI. Conclusion

A new multilevel single-stage AC–DC converter is proposed in the paper. This converter is operated with two controller's one controller that performs input PFC and a second controller that regulates the output voltage. The outstanding feature of this converter is that it combines the performance of two-stage converters with the reduction of cost of single-stage converters. The paper introduces the proposed converter, explains its basic operating principles and modes of operation, and discusses its design with respect to different DC-bus voltages. Experimental results that confirm the feasibility of the converter are also presented in the paper.

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