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# DESIGN AND ANALYSIS OF REVERSIBLE VEDIC MULTIPLIER IN NANO SCALE TECHNOLOGY

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***Abstract— The multipliers based on Vedic mathematics are one of the low power and fastest multiplier. It enables parallel generation of partial product and eliminates unwanted multiplication steps. Reversible logic is one of the most emerging technologies in low power VLSI circuits. Reversible gates are the gates that the numbers of inputs provides output which is applied to another gate whose output is equal to the initial input. Reversible logic circuits have many applications in reversible computing, quantum computing, quantum dot cellular automata, optical computing and low power design. In spite of this irreversible, reversible circuits are not power dissipated, thus they are significant. This is accomplished by revamping the partial product formation architecture. The technique effectively forms the entire partial product. In this paper a reversible multiplier is designed with the help of multiplier by using reversible gates. Thus results improve quantum cost and reduce the garbage outputs.***

***Index Terms— Quantum cost, Quantum computing, Garbage output. Vedic Multiplier.***

## I. INTRODUCTION

Multipliers are the fundamental and essential building blocks of VLSI systems. The design and implementation approaches of multipliers contribute substantially to the area, speed and power consumption of computational intensive VLSI systems. Often, the delay of multipliers dominates the critical path of these systems and due to issues concerning reliability and portability, power consumption is a critical criterion for applications that demand low-power as its primary metric. While low power and high speed multiplier circuits are highly demanded, it is not always possible to achieve both criteria simultaneously. Therefore, a good multiplier design requires some tradeoff between speed and power consumption.

The word "Vedas" which literarily means knowledge has derivational meaning as principle and limitless store-house of all knowledge. The word Veda also refers to the sacred ancient Hindu literature which is divided into four volumes. Vedas are considered to be one of the oldest forms of written records by man. Vedas initially were passed from previous generations to next orally. Later they were transcribed in Sanskrit. A survey of all scripts available of Vedas across different part of India showed no slightest difference in them. Vedas include information from many subjects from religion, medicine, architecture, astronomy, mathematics etc.Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). A scholar from India Shri Bharati Krishna Tirthaji after careful study of appendix of one of the Vedas – Atharvaveda, reconstructed a mathematical system based on the formulas in it. The main purpose of the system was to use some techniques to solve the lengthy mathematics orally or with minimum space utilization on paper. The system of Vedic mathematics is based on 16 Sutras.

The general intent computing automation is logically unalterable. In such machine may be made by logically revocable.laudauer proved heat generation requires a negligible heat generation per machine cycle. For each revocable function of kTln2 [1]. Where k = 1.3806505x10-23J/K is Boltzmann constant and T is the operating temperature in Degrees. The reversible computer which performs useful computation .The logically revocable automation parallels the corresponding unalterable operation. This is consisting of print the desired output. Landauer principle every computation some amount of energy was unavoidable, but Bennett proves in the reversible condition kTln2 energy was not avoidable .This is also have three stage of served function. In the deterministic automaton finite or infinite granted it sufficient storage to record the history [2]

Reversible logic is mainly emerging fast growing in research topic, having applications in many fields such as low power design, optical processing and quantum computation.

## II.BASIC REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic

device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits. Reversible if there is a one-to-one correspondence between its input vector and output vector. In the reversible circuits, not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs.

Feynman Gate :

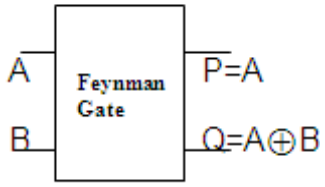


Fig 1

Toffoli Gate :

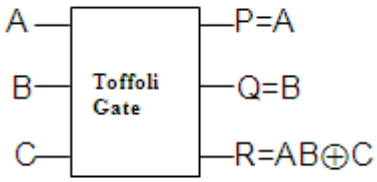


Fig 2

The reversible 2*2 gate with quantum cost of one having mapping input (A, B) to output (P = A, Q = A⊕B) is asshown in the fig-1

The 3*3 reversible gate with three inputs and three outputs.The inputs (A, B, C) mapped to the outputs (P = A, Q = B, R = AB⊕C) is as shown in the fig-2

Fredkin Gate :

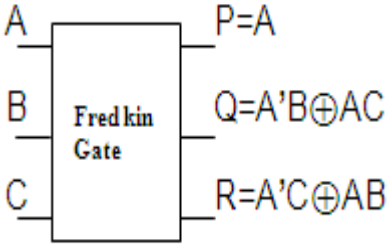


Fig 3

Reversible 3*3 gate maps inputs (A, B, C) to outputs (P = A, Q = A'B⊕AC, R = A'C⊕AB) having quantum cost of five) is as shown in the fig-3

Peres Gate :

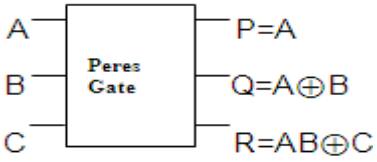


Fig 4

The three inputs and three outputs i.e., 3*3 Reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A⊕B, R = (AB) ⊕C). ) is as shown in the fig-4.

Double Peres Gate :

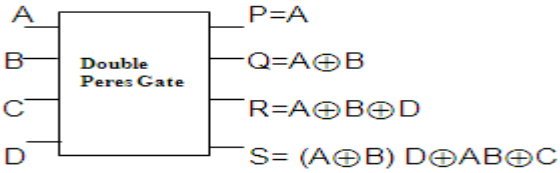


Fig 5

The 4x4 reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to (P = A, Q = A⊕B, R = A⊕B⊕D, S = (A⊕B) D⊕AB⊕C) is as shown in fig-5.

## III BACKGROUND WORK

Himanshu Thapliyal and Srinivas [4] proposed an NxN reversible multiplier using TSG gate. In this the partial products are generated using Fredkin gates and addition using reversible parallel adder designed from TSG gates and demonstrated that the multiplier architecture using TSG gate is optimized. Majid Haghparast et al., [5] presented two new 4x4 bit reversible multiplier designs which have low hardware complexity, less garbage input/output bits and less quantum cost and implementation of reversible HNG is also presented. Noor Muhammed Nayeem et al., [6] explained the use of reversible logic for designing the Arithmetic Logic Unit of a crypto processor. A reversible carry save adder using modified TSG gates and architecture of Montgomery multipliers are also discussed. Maryam Ehsanpour et al., [7] explored the reversible 4-bit binary multiplier circuit using new reversible device called modified full adder with low hardware complexity, fewer garbage outputs and constant inputs. Himanshu Thapliyal and Nagarjan Ranganathan [8] proposed a design of reversible BCD adder which is primarily optimized for the number of input bits and number of garbage outputs, results in the reduction of quantum cost and the delay. Himanshu Thapliyal and Nagarjan Ranganathan [9] presented the design of the reversible half

and full subtractor based on the quantum gate implementation of the reversible TR gate. The reversible half and full subtractor shown better in terms of the quantum cost, delay and minimum number of garbage outputs.

## IV PROPOSED MULTIPLIER

The proposed 4X4 reversible gate called Toffoli, Peres and DPG gate is shown in fig-2, 4 & 5.

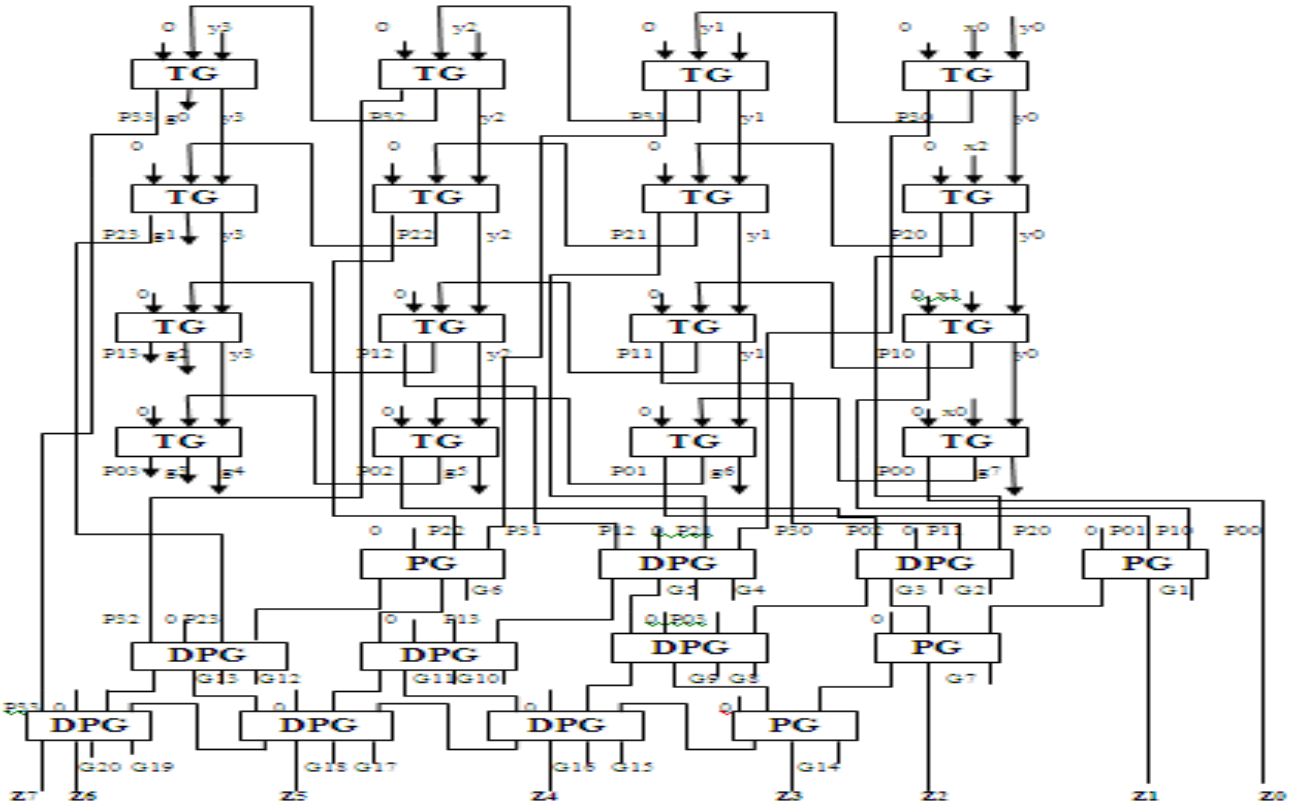


Fig 6

A reversible multiplier has two sections

- Partial Product Generation (PPG) circuit
- Multi-Operand Addition (MOA) circuit

### A. Partial Product Generation

The basic operation of 4x4 parallel multiplier, It consists TG gate is depicted in fig-7

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | X3 | X2 | X1 | X0 |
| | | | | Y3 | Y2 | Y1 | Y0 |
| | | | | X3.Y0 | X2.Y0 | X1.Y0 | X0.Y0 |
| | | | X3.Y1 | X2.Y1 | X1.Y1 | X0.Y1 | |
| | | X3.Y2 | X2.Y2 | X1.Y2 | X0.Y2 | | |
| | X3.Y3 | X2.Y3 | X1.Y3 | X0.Y3 | | | |
| Z7 | Z6 | Z5 | Z4 | Z3 | Z2 | Z1 | Z0 |

Fig 7

B. Multi-Operand Addition

The addition of the partial products using DPG and PG gates is as shown in figure 7

## V SIMULATION OUTPUT

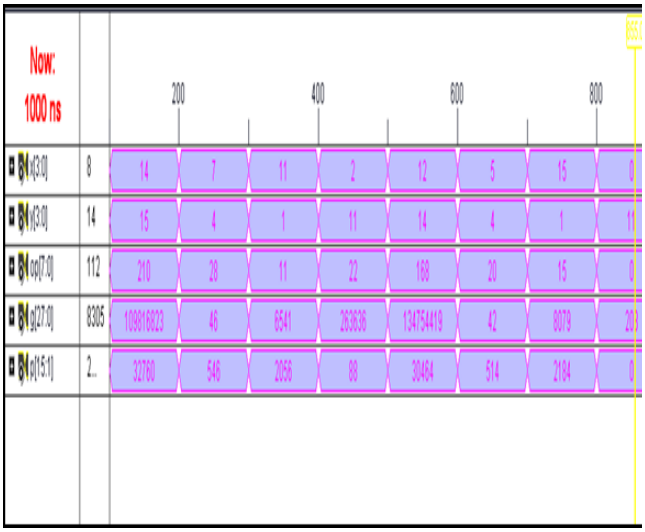


Fig 8

Comparison with existing reversible multiplier design.

| *Designs* | *Gate count* | *Constant inputs* | *Garbage outputs* | | | | |
|---|---|---|---|---|---|---|---|
| Proposed design | **28** | **28** | **28** | | | | |
| Existing design[10] | **32** | **40** | **40** | | | | |

Table 1

## VI CONCLUSION AND FUTURE WORK

An efficient reversible multiplier is designed by using reversible gates. Compared to the best of other existing designs, the proposed reversible multiplier provides less delay with reduction in gate counts and Constant inputs. Future work involves, an effective reversible Vedic multiplier is designed by using Vedic Mathematics with the performance measures such as delay, gate count, constant inputs, and power and garbage outputs.

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