International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)
ISSN: 0976-1353 Volume 24 Issue 2 – FEBRUARY 2017.

Enhanced Memory Reliability for Correcting Cell Upsets With Reduced Redundancy

Sridharraj S[#1], Abirami AP[*2]and Akashni A[*3]

[#] *Assistant Professor, Dept. of ECE, Mepco Schlenk Engineering College, Sivakasi, TN, India*

[*] *UG students, Dept. of ECE, Mepco Schlenk Engineering College, Sivakasi, TN, India*

***Abstract*—Memories are one of the key elements in any electronic systems. Multiple Cell Upsets (MCU) poses a great threat to the reliability of memories which are exposed to radiation. Due to the increasing demands in the application of satellite communication field the devices are exposed to very wide range of environmental radiation. More complex error correction codes (ECC) are proposed widely to overcome data corruption but the problem they face is that they require higher delay overhead. Recently, Decimal Matrix Codes (DMC) based on hamming codes have been proposed for the protection of memories. In this paper, DMC based on divide-symbol algorithm has been proposed to enhance memory reliability. A less number of redundant bits to be stored and a minimized delay overhead in data correction are always the best method to implement an error correction code. Encoder Reuse Technique (ERT) uses DMC encoder itself to be the part of decoder, thus minimizes the area overhead of extra circuits. The only drawback of existing MC is that more number of redundant bits are required to maintain higher reliability of memory. The proposed technique presents an FPGA based execution of memory data error detection and correction using DMC and another technique called Parity Matrix Code (PMC) to assure reliability in presence of MCU and to reduce redundant bits and increases error correction capability.**

***Keywords*—Multiple Cell Upsets(MCU),Decimal Matrix Code(DMC),Parity Matrix Code(PMC),Memory.**

I. INTRODUCTION

The increasing rates of embedded memories in electronics system that are exposed to environmental radiations especially in space due to ionizing effects of neutrons, alpha particles etc., are the main reason for the rapid increase of soft error rate in recent times. The error generation due to radiation effect in the memories that are exposed to environmental radiations are shown in Fig. 1.

Eventhough, single bit upset is one of the major concerns about memory reliability, multiple cell upsets have become seriou reliability concern in recent memory applications. Idea that is used for error detection and correction is done by adding extra bits(i.e., redundant bits) from which the receiver will be able to locate the error and correct them. Error detection and correction can be either schematic or non-schematic: In schematic scheme, unique data acts as input along with the additional check bits that are determined by some specific algorithm. For the purpose of error detection, the receiver can use the same algorithm to received data and compares its output to the check bits. If the values do not match then the error can be detected in that specific location. In a system that uses non-systematic scheme, the incoming message is converted to an encoded data which has at least many bits as the unique message. Some of the error correction codes (ECCs) techniques have been widely used to protect memories and make it as fault-tolerant as possible for years. Previously, Bose Choudhary-Hocquenghem (BCH) code, Reed-Solomon (RS) code and Punctured Difference Set (PDS) code have been used to deal with MCUs in memories. But these codes have their encoding and decoding circuits more complex, thus require more area, power and delay overhead. Hamming codes are used to correct Single Error Upsets (SEUs) due to their ability to correct only single errors through reduced area and performance overhead. But they cannot correct double bit errors caused in single event. An extension of basic Single-error-correcting and Double-error-detecting (SEC-DED) Hamming codes has been proposed to form special type of codes known as Hsiao Codes to increase the speed, cost and reliability. Another class of SEC-DED codes known as Single-error-correcting, Double-error-detecting and Single-byte-error-detecting SEC-DED-SBD codes have been proposed to detect any number of errors. Interleaving leaving technique has been used to restrain MCUs, that rearranges cells in physical arrangement to separate the bits in the same logical word to different physical words. But this interleaving cannot be performed practically in Content-addressable memory (CAM) because of the hardware structures of both cells and comparision circuits.

Built-In-Current Sensors (BICS) are proposed along with SEC-DED codes to provide protection against MCUs. However, it can correct only upto two bit errors. MCUs per word can be efficiently corrected by 2D-Matrix codes. In 2D-MC, one word is divided into multiple rows and multiple columns. This code has minimum overhead delay when

compared to others. This paper proposes decimal matrix code (DMC) based on divide-symbol algorithm to provide enhanced memory reliability. The Exisiting DMC uses decimal algorithm (decimal integer addition and subtraction) which haa an advantage of enhanced memory reliability and maximization of error detection and correction capability. But it requires more redundant bits. The Proposed method reduces the need for extra bits that are required to detect errors.

This paper is arranged as follows: section-II presents some of the previous work done by the research scholars under the title 'Literature Review'. Section-III presents the design of existing DMC architecture and also the design of proposed DMC architechture. Section-IV presents the proposed PMC design to correct errors with reduced redundancy. Simulation results are presented in the section-V. Finally, Conclusion of this paper is given in the Section-VI.

II . LITERATURE REVIEW

In [1], DMC was proposed to prevent multiple cell upsets (MCUs) in memory, so that more than one error can be corrected. A comparative study of various error correction code is discussed in [2] and this approach overcomes the reliability issue. In the reference paper [3] and [4], some of the new techniques have been discussed using hamming codes for the correction and reliability of memories. Knowledge on the extension of single-error correction and double-error detection (SEC-DED) codes are obtained from [5]. In reference [6] and [7], data protection using DMC in CAM cells are proposed. Carry Save Adder based decimal error detection technique is implemented in the reference [8]. Single-error correction, double-error detection, triple adjacent error detection (SEC-DED-TAED) codes are proposed in the references [9] and [10], that uses efficient extended hamming codes to correct single bit errors and detect large number of double & triple adjacent errors (DAED & TAED). The next level protection of memory is shown in [11], that provides increased capability of error detection using Hybrid Matrix Code (HMC). In the reference [12], the cost efficient scheme based on erasure codes for MCU detection and correction in the configuration schemes of SRAM-based FPGA is presented. In the reference [13], advantages of using PMC for the error detection and correction is explained in detail. In the reference [14], the reliability and security of the data stored in memory is improved and the Encoder Reuse Technique (ERT) based DMC implementation is performed to reduce the area of the design explained.

III . DESIGN OF DECIMAL MATRIX CODE

In this section, DMC was designed with encoder and decoder in order to assure reliability in memory. Here 32 bit word is encoded and decoded as an example for the existing DMC technique.

A. Schematic of Fault Tolerant Memory

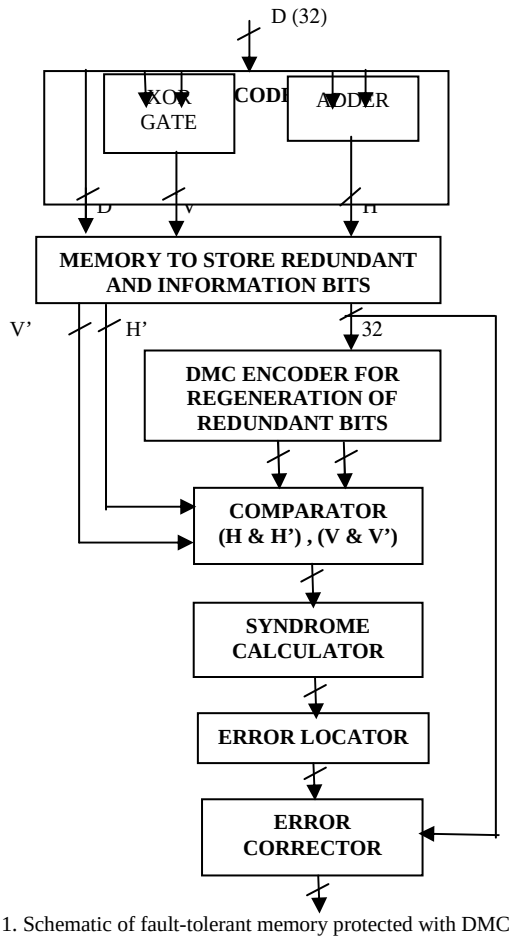

Fig 1. Schematic of fault-tolerant memory protected with DMC

The schematic of the existing fault-tolerant memory is shown in Fig. 1. Initially, encoding process takes place where input data is fed into the DMC encoder. The horizontal (H) and vertical (V) redundant bits are calculated from the encoder. Once the process inside the encoder is complete, the information is made to store inside the memory. When MCUs take place in the memory, the errors can be corrected in the decoding process. ERT technique is used, thus there is no need of area for extra circuits in the decoder. The major drawback of existing system is that it requires more redundant bits for the detection and correction of data.

B. Existing DMC Encoder

In DMC, first, Divide-Symbol algorithm is used and performed using arrange-matrix ideas, i.e., N -bit word is divided into k symbols of m bits each ($N = k$ x m) and these are arranged as 2D-matrix ($k = k_1$ x k_2, where k_1 and k_2 are the no. of rows and columns respectively in the logical matrix). Next, Horizontal redundant bits are obtained by performing decimal addition of selected symbols per row. Here, each symbols is considered as an integer value. Then, the vertical redundant bits are

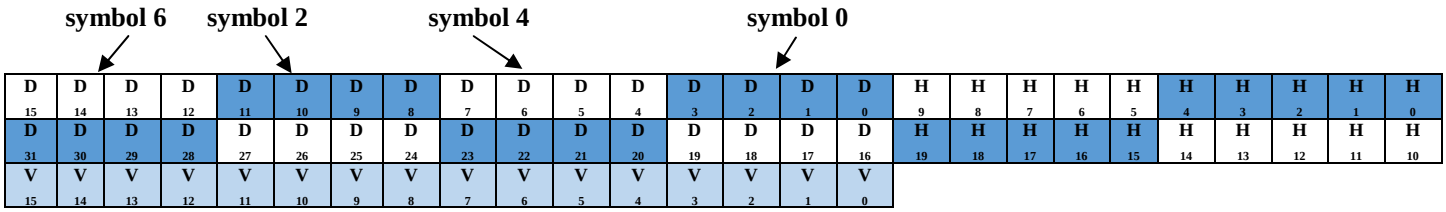

Fig. 2. Logical organisation of existing 32-bit DMC design

obtained by xor –operation among the bits per column. Main thing to be noted here is that, divide-symbol algorithm and matrix ideas are performed only logical without causing any changes in the physical structure of memory.

In order to explain the DMC scheme, 32-bit word is taken as example. Here, k and m should be carefully chosen so that it meets the requirement of memory reliability, maximum capability of error correction and minimum redundant bits. For the purpose of enhanced memory reliability, k= 2 x 4 and m= 4 are considered. Logical organisation with k=2x4 and m=4 is shown in Fig. 2. Here, the input 32 bit word considered is divided into eight symbols of four bits each. H_0-H_{19} is considered as horizontal redundant bits and V_0-V_{15} is considered as vertical redundant bits, so totally 36 redundant bits are required.

The H can be obtained by decimal integer addition as follows:

$$H_4H_3H_2H_1H_0 = D_3D_2D_1D_0 + D_{11}D_{10}D_9D_8 \quad (1)$$
$$H_9H_8H_7H_6H_5 = D_7D_6D_5D_4 + D_{15}D_{14}D_{13}D_{12} \quad (2)$$
$$H_{14}H_{13}H_{12}H_{11}H_{10} = D_{19}D_{18}D_{17}D_{16} + D_{27}D_{26}D_{25}D_{24} \quad (3)$$
$$H_{19}H_{18}H_{17}H_{16}H_{15} = D_{23}D_{22}D_{21}D_{20} + D_{31}D_{30}D_{29}D_{28} \quad (4)$$

For the calculation of V we have the following procedure:

$$V_0 = D_0 \oplus D_{16} \quad (5)$$
$$V_1 = D_1 \oplus D_{15} \quad (6)$$

Thus, the equation from (1) to (6) can be used to perform encoding operation. The encoder that computes horizontal and vertical redundant bits are shown in Fig. 3. From the figure, H_0-H_{19} are horizontal redundant bits, V_0-V_{15} are vertical redundant bits and U_{31}-U_0 are information bits.

C. Existing DMC decoder

In order to correct the word that is corrupted, we find the need to go for decoder. First, the same encoding process is done in the decoder for the generation of horizontal (H_0'-H_{19}') and vertical (V_0'-V_{15}') redundant bits of corrupted data D'. Next, the syndrome calculation is done for both horizontal and vertical redundant bits.

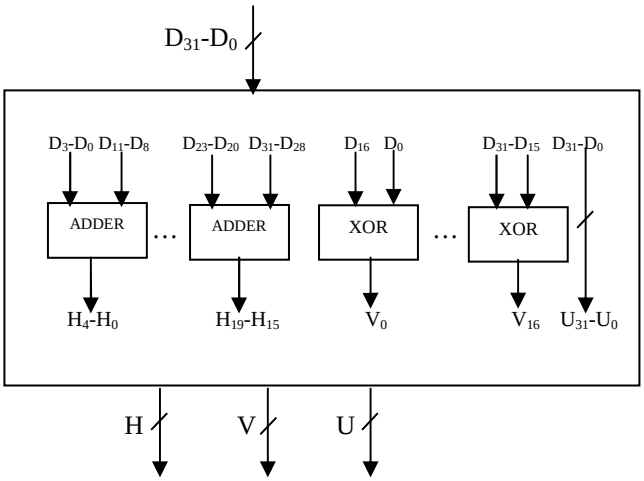

Fig. 3. 32 bit Existing DMC Encoder using multibit adders and xor gates

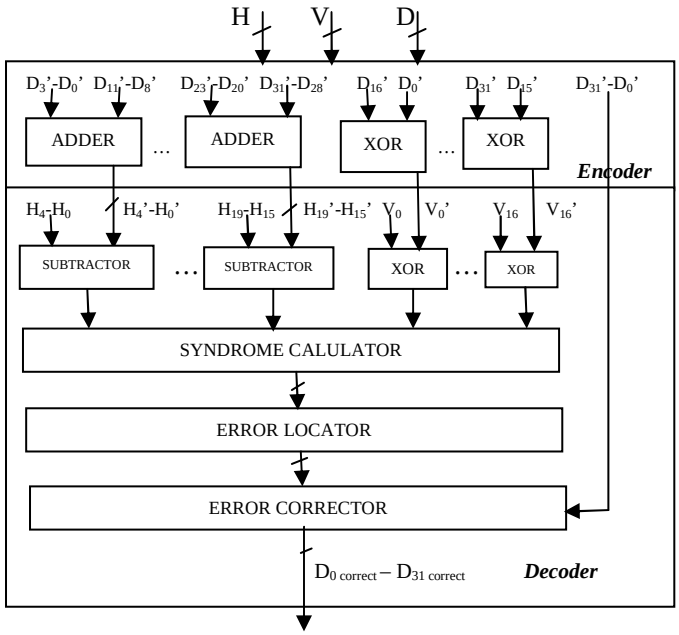

Fig. 4. Existing DMC decoder using ERT

$\Delta H_4H_3H_2H_1H_0 = H_4'H_3'H_2'H_1'H_0' - H_4H_3H_2H_1H_0$ (7)

$S_0 = V_0' \oplus V_0$ (8)

The equation (7) and (8) can be used to find every syndrome bits. When $\Delta H_4H_3H_2H_1H_0$ and S_3-S_0 are zero, then there is no error in symbol 0. If they are not equal to zero, then error can be located in symbol 0, and the errors can be corrected using the following formula:

$D_0 = D_0' \wedge S_0$ (9)

The DMC decoder is shown in Fig. 4. It consists of submodules syndrome calculator, error locator and error corrector. From the figure, the redundant bits for the corrupted data D' is computed and then compared with the redundant bits of original data to obtain syndrome bits ΔH and S.

The syndrome bits calculated are used to locate the errors that occurred and finally in error corrector, the errored bit can be corrected by inverting the value. In this DMC scheme, circuit area is reduced by using ERT technique. From figure Fig. 4, it is seen that encoder is reused in the decoder. Therefore, the area of DMC is reduced as a result of existent circuits of encoder. But the only drawback in the existing technique is that they require more redundant bits in order to locate the error.

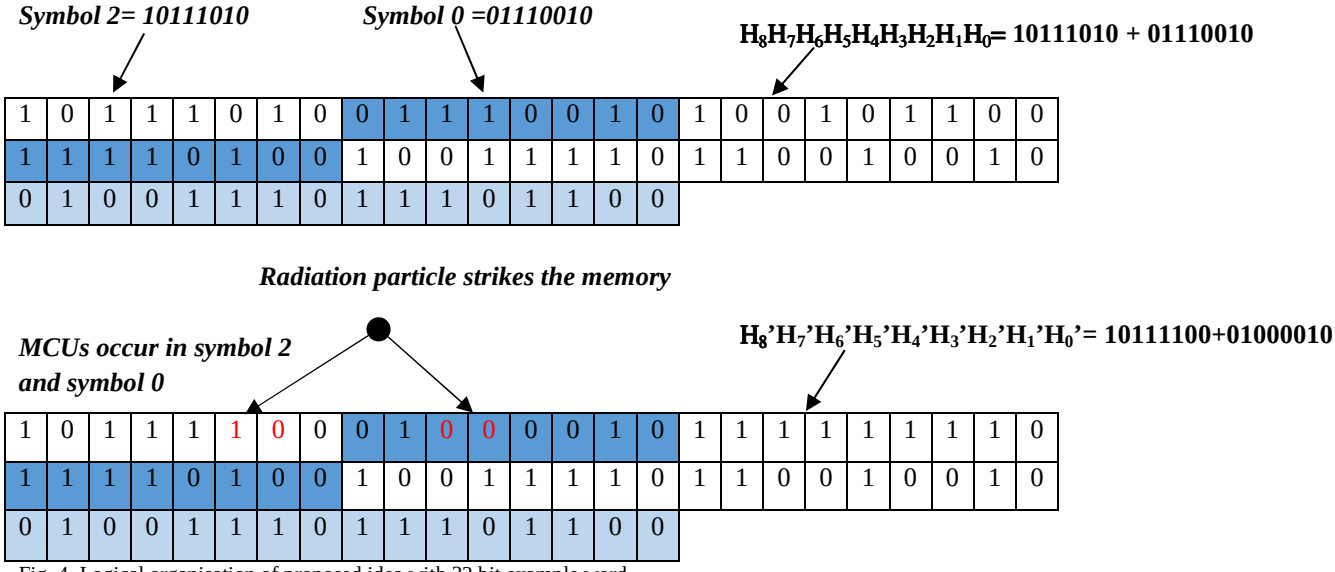

Fig. 4. Logical organisation of proposed idea with 32 bit example word

In order to overcome the drawbacks in the existing model, new technique of DMC was proposed to reduce the redundancy used to detect and correct the errors, thus highly effective than the existing technique.

D. Proposed DMC encoder and decoder

The proposed design of DMC encoder and decoder reduced the number of extra bits used, thus rectified the drawback of existing system. In the proposed DMC encoder, k= 2 x 2 and m=8 is chosen to enhance the memory reliability, increase the error correction capability and also minimize the redundant bits than the existing system. The procedure and operation of the proposed encoder and decoder is same as that of existing but it differs only in the logical organisation of input 32-bit word. The logical organisation of the proposed idea is shown in the Fig. 4.

Here, the 32-bit word is divided into four symbols of eight bits each. In Fig. 4. H_0 – H_{17} are horizontal redundant bits and V_0-V_{15} are vertical redundant bits, so only 34 redundant bits are required. First, in the encoder, horizontal redundant bits are calculated using the following formula:

$H_8H_7H_6H_5H_4H_3H_2H_1H_0=D_7D_6D_5D_4D_3D_2D_1D_0+D_{15}D_{14}D_{13}D_{12}D_{11}D_{10}D_9D_8$ (10)

Similarly, H_9-H_{17} can be calculated. The vertical redundant bits calculation is same as that of existing DMC encoder. Next in DMC decoder, horizontal redundant bits (H_0'-H_{17}') for the corrupted data is calculated with the same encoding process. And the procedure for finding syndrome bits are done as the previous method.

$\Delta H_8H_7H_6H_5H_4H_3H_2H_1H_0 = H_8'H_7'H_6'H_5'H_4'H_3'H_2'H_1'H_0' - H_8H_7H_6H_5H_4H_3H_2H_1H_0$ (11)

$S_0=V_0'\oplus V_0$ (12)

The equation (11) and (12) can be used to find remaining syndrome bits. When $\Delta H_8H_7H_6H_5H_4H_3H_2H_1H_0$ and S_7-S_0 are zero, then there is no error in symbol 0. If they are not equal to

zero, then the error can be located in the symbol 0. Similarly, errors in every symbol can be located using this procedure and they can be corrected using the following formula

$$D_0 = D_0' \oplus S_0 \quad (13)$$

In this proposed scheme, the drawback of the previous design was rectified and the error correction capability is also maximized. Here, we required only 18 horizontal redundant bits. Considering 32 bit word as an example, the process of error detection is explained in the logical organisation explained in Fig. 4. The proposed DMC can correct any types of single bit error and multiple-error correction in two consecutive symbols. It can correct up-to 16-bits of upsets.

IV. PROPOSED DESIGN OF PMC

In this section, Parity Matrix Code (PMC) based encoder and decoder design are described. This has greater advantage than DMC in the reduction of redundant bits.

A. PMC encoder

In PMC, first, divide-symbol algorithm and arrange matrix techniques are performed as that of DMC. Similar to the DMC, the N-bit word is divided into k symbols of m-bits each. Here, k= k_1 x k_2, where k_1 and k_2 are the number of rows and columns in logical organisation respectively. Then, the horizontal redundant (H) bits are calculated by performing 7:4 hamming encoding of selected symbols in first row. Then, the vertical redundant bits (V) are obtained by binary operation of bits in both the rows.

In order to explain PMC scheme, 32-bit word is taken as an example as shown in Fig. 5. The cells from D_0-D_{31} is information bits. The 32-bit word is divided into eight symbols of each 4 bits. In the logical organisation shown in Fig. 5. , the first consist of information from D_0-$D_{15.}$ The horizontal check bits (H_0-H_{11}) are obtained only for the first row. V_0-V_{15} are vertical redundant bits. The number of redundant bits are different when different values of k and m are chosen. Hence, k and m should be carefully chosen to increase the correction capability and reduce the requirement of redundant bits. In this paper, k = 2 x 4 and m= 4 is chosen so that redundant bits are reduced to 28 and correction capability is also increased.

The horizontal redundant bits (H) are obtained by hamming (7, 4) coding. For the calculation of H, first we need to calculate check bits. For example, consider symbol 0 ($D_0D_1D_2D_3$) as integer. The check bits C_0, C_1, C_2 can be generated from the following equations:

$$C_0 = D_3+D_2+D_1 \quad (14)$$
$$C_1 = D_3+D_1+D_0 \quad (15)$$
$$C_2 = D_0+D_1+D_2 \quad (16)$$

If C_0 is even, H_0 is zero else it is one. If C_1 is even, H_1 is zero else it is one. If C_2 is even, H_2 is zero else it is one. Similarly, remaining horizontal bits can be obtained from the remaining symbols. Vertical redundant bits are obtained using the following formulas:

$$V_0=D_0 \wedge D_{16} \quad (17)$$

Similarly, rest of the vertical redundant bits are calculated.

B. PMC decoder

In order to obtain the original data, we go for decoding process. First, the horizontal redundant bits (H_0'-H_{11}') and vertical redundant bits (V_0'-V_{15}') are calculated for the received information bits D'. Next, the horizontal and vertical syndrome bits are obtained using the following formulas:

$$\Delta H_2H_1H_0 = H_2'H_1'H_0' - H_2H_1H_0 \quad (18)$$
$$S_0=V_0' \oplus V_0 \quad (19)$$

And the rest of the syndrome bits are generated using the formulas (18) and (19).

When $\Delta H_2H_1H_0$ is zero, then the stored information in symbol 0 is error free, if it is not equal to zero, then there is error in symbol zero and by checking vertical redundant bits which is not equal to zero, the errored value can be detected and corrected using the following formula:

$$D_{0\ correct} = D_0 \oplus S_0 \quad (20)$$

The equation (20) can be used to correct errors in other locations. In PMC, ERT technique is used as that of DMC in order to minimize circuit area without disturbing the encoder and decoder process.

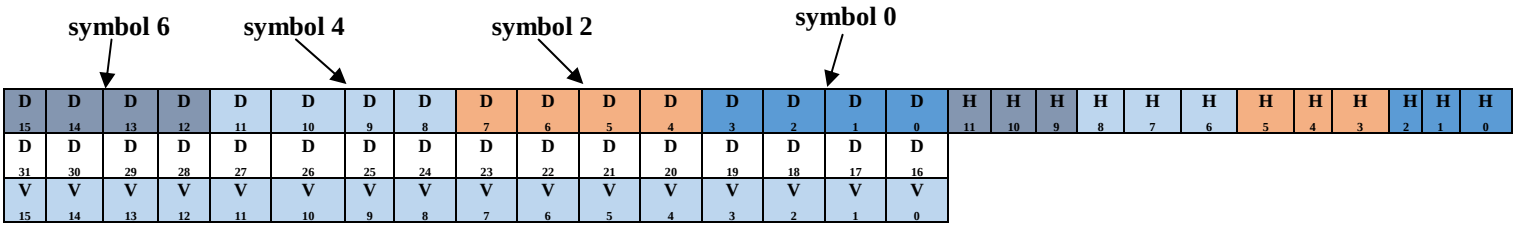

Fig. 5. PMC organization for 32-bit word

V. SIMULATION RESULTS

The simulation is carried out using MODELSIM ALTERA STARTER EDITION 6.4a. The simulation results for existing DMC technique, proposed DMC technique and the proposed PMC technique is shown in fig.6, fig.7, fig.8 respectively as a screenshot taken from above mentioned software.

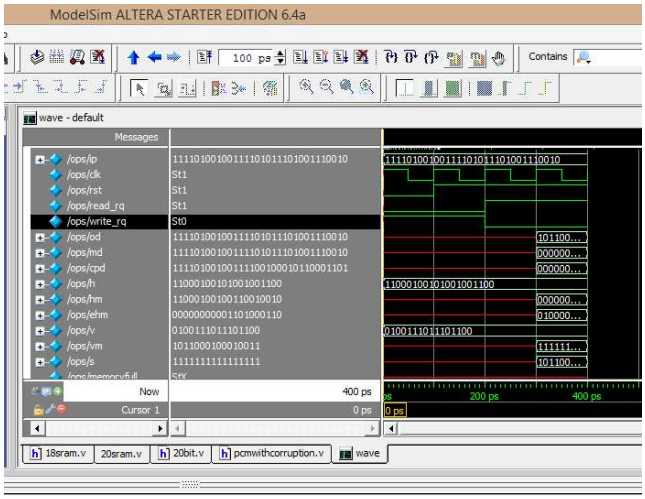

Fig.6 simulation result for existing DMC techniue

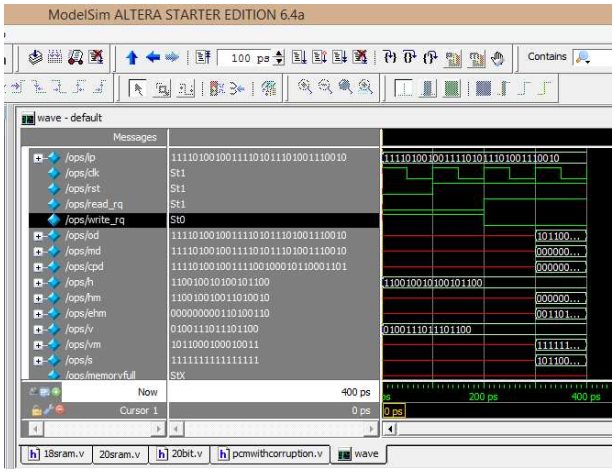

Fig.7 simulation result for proposed DMC technique

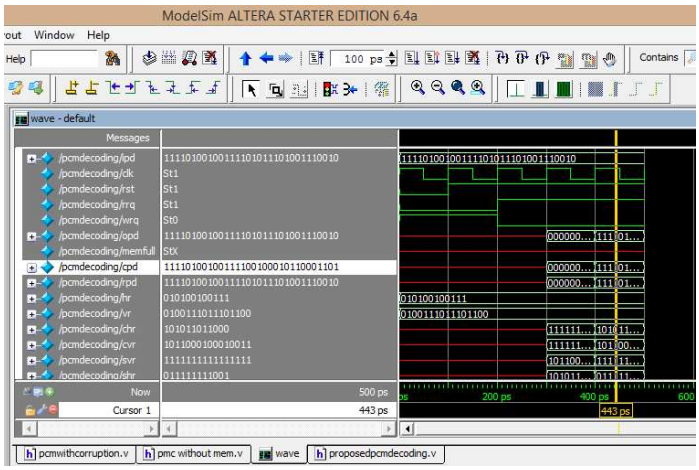

Fig.8 simulation result for proposed PMC technique

Table 1. gives the comparison of existing DMC, proposed DMC and PMC technique.

TABLE 1: COMPARISON OF DMC AND PMC

Parameters	Existing DMC	Proposed DMC	Proposed PMC
No. of errors corrected	12 bit	16 bit	16 bit
No. of redundant bits	36 bit	34 bit	28 bit

VI.CONCLUSION

This paper dealt with three techniques in order to reduce redundant bits used for fault tolerant memory. Two types of error correction codes Decimal Matrix Codes (DMC) and Parity Matrix Codes (PMC) are discussed in detail. DMC used decimal algorithm to improve error correction capability. And moreover ERT technique was proposed to minimize the area overhead of extra circuits without disturbing the whole process. The existing DMC technique had the drawback of more number of redundant bits. This drawback was rectified in the proposed DMC technique thus reducing the no. of redundant bits used. But the use of PMC can reduce the redundant bits further. The proposed PMC technique of error correction and detection has increased the error correction capability and the no. of redundant bits are reduced. Encoder Reuse Technique (ERT) is also utilized in PMC, thus considering PMC highly advantageous than other techniques.

REFERENCES

[1] Jing Guo, Liyi Xiao, Member, IEEE, Zhigang Mao, Member, IEEE, and QiangZhao,"Enhanced memory reliability against multiple cell upsets using Decimal Matrix Code" IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., vol. 22, no. 1, pp.127-135, Mar 2013.

[2] David S, and Gayathree K., "A Comparative Study of Various Error Correction Codes", International Journal of Computer Science and Mobile Computing (IJCSMC), Vol.3 Issue 8, pp.196-200, August 2014.

[3] Kamalakannan S, Karthikeyan S, Sathyamoorthy K, "Implementation of Error Correction Technique Based on Decimal Matrix Code", International Journal of Advanced Research Trends in Engineering and Technology (IJARTET), Vol.2 Issue 4, April 2015.

[4] Madhuri K, Thrimurthulu V, "Implementation of decimal matrix code for correcting cell upsets in SRAM", International Journal of Electrics, Electronics and Data communication, ISSN:2320-2084 Vol-2, Issue 10,October-2014.

[5] M.Y. Hsiao, "A class of Optimal Minimum Odd-Weight-Column SEC-DED Codes"

[6] K pagiamtzis, A sheikholeslami. "Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey", IEEE J. Solid State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2003.

[7] S. Baeg, S. Wen, and R. Wong, "Minimizing soft errors in TCAM devices: A probabilistic approach to determining scrubbing intervals," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 814–822, Apr. 2010.

[8] K. Janani and R. Ponni, "FPGA based protection of Soft Errors using Multiple Error Correction Codes", IJESC, January 2015.

[9] A. Sanchez-Macian, P. Reviriego, and J. A. Maestro, "Hamming SECDAED and extended hamming SEC-DED-TAED codes through selective shortening and bit placement," IEEE Trans. Device Mater. Rel., to be published.

[10] Sandyarani K, Nirmal kumar P,"Extenden hamming SEC-DAED-TAED based Fault Detection Technique for AES encryption and decryption", Indian Journal of Science and Technology, vol9(33), September 2016.

[11] Maria Antony S. and Sunitha K., "Hybrid Matrix Codes for Enhanced Memory Reliability against Multiple Cell Upsets", International Journal for Scientific Research and Development (IJSRD), Vol.3 Issue 1, pp.114-117, January 2015.

[12] Aishwarya S, Mahendran G, "Multi Bit Upset correction in SRAM based FPGA using self repairable Erasure codes", International Conference of Emerging Trends and Science (ICEETS-2016).

[13] Gayathree K, David S, Moortheeswari M, "Reliability Enhancement Using Parity Algorithm", International Journal of Innovative Science, Engineering & Technology, Vol.2 Issue4, April 2015.

[14] Gayathree K, David S, "Analysing the Power Overhead of Decimal Matrix Code With Different Adder Architecture", International Journal of Research in Engineering and Advanced technology, Vol.3 Issue 2, April-May 2015.