International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)
ISSN: 0976-1353 Volume 24 Issue 4 – MARCH 2017.

PERFORMANCE EVALUATION OF 4:1 MULTIPLEXER USING DIFFERENT DOMINO LOGIC

Harishripriya.M[#1], Kavitha.R [#2] and Vengadapathiraj.M [*2]

[#] *Student, Electronics and Communication Engineering, Rajalakshmi Institute of Technology, Chennai, India*

[*] *Assistant professor, Electronics and Communication Engineering, Rajalakshmi Institute of Technology, Chennai, India*

***Abstract*— In the current scenario, the low power, high speed and area plays a vital role in the field of digital VLSI circuits. The major challenge in VLSI circuits is to obtain high performance. Objective of this paper is to design a 4:1 Multiplexer with using various domino logic techniques. The main emphasis of this work is to find the best probable trade off that would enhance multiple goals viz. area, power, speed. The outcome of this paper is simulated on the EDA tanner tools realized in 0.25-micrometer technology.**

***Index Terms*— Multiplexer, domino logic, Low power, Inverter feedback technique, domino keeper technique.**

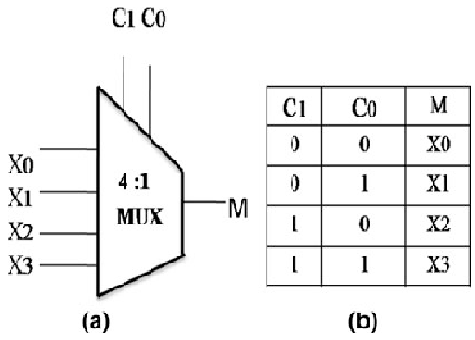
I. INTRODUCTION

In the present situation, effective utilization of power plays an vital aspect in digital VLSI circuits, different techniques are used to design circuits for low power consumption with high speed interface applications are developed. Multiplexing method is premeditated to shrink the number of electrical connections in the display matrix, whereas driving signals are functional not to each pixel individually but to a group of rows and columns at a time. In addition reducing the number of independent interconnections, multiplexing also simplifies the drive electronics, reduces the rate and provides direct interface with the microprocessors. There are margins in multiplexing due to complex electro-optical retort of the liquid crystal cell. In this paper, 4:1multiplexer has been designed using various domino logic with low power consumption and higher packing densities and these implementations are based on power consumption in 0.25mm technology.

II. MULTIPLEXER

Multiplexer is a combinational logic circuit that selects one of several digital input signals and forwards the selected input into a single line. Multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. The multiplexer sometime is called date selector.

The graphical symbol and switching operation of 4:1multiplexer is shown in Figure1. The final result of 4:1 multiplexer appears in the below table for various facts situations.



C1	C0	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

Figure1: Graphical Symbol and Switching Operation of a 4:1 Multiplexer Logic

Expression for multiplexer output is given as,

$$M = \overline{C1}\ C0\ X0 + C0\ C1\ X1 + \overline{C0}\ C1\ X2 + C0\ C1\ X3$$

If 4 inputs I_0, I_1, I_2, I_3 is given with selection lines S_1 and S_0, the logic circuit diagram is

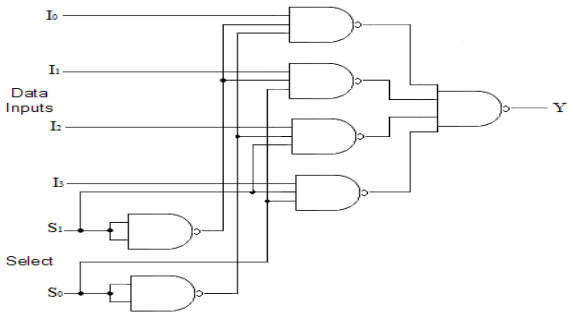


Figure 2: Logic diagram of MUX

III. PRECHARGE AND EVALUATION PHASE OF DOMINO LOGIC IN 4:1 MUXTIPLEXER

Domino logic is the most popular dynamic logic. It is nothing but a CMOS circuit with clock signal.In Basic, Domino logic family evolved from PMOS and NMOS

transistors and therefore retained two phase of operation, the first phase is set up phase or pre charge phase. In this phase, the clock signal is low (clk=0) and the output goes unconditionally (no matter the values of the inputs A and B). Therefore the capacitor which represents the load capacitance of this gate becomes charged.

Next, during the evaluation phase the clock is high (clk=1). In this stage the output node may be discharged if inputs have arranged a directing path to ground, else the output node stays charged high. Before the clock pulse goes high the Inputs must be stable because once the output has been discharged it won't go high again until the succeeding cycle.

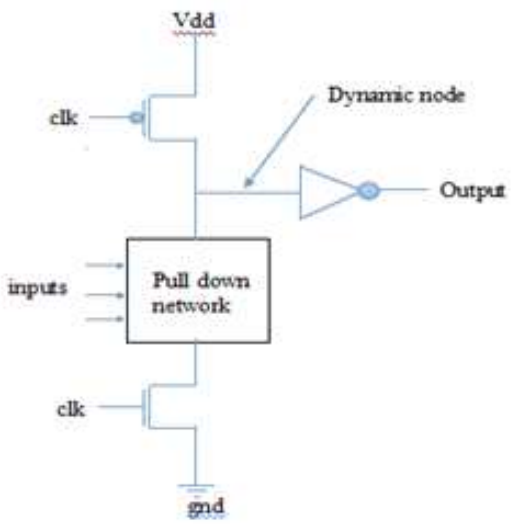
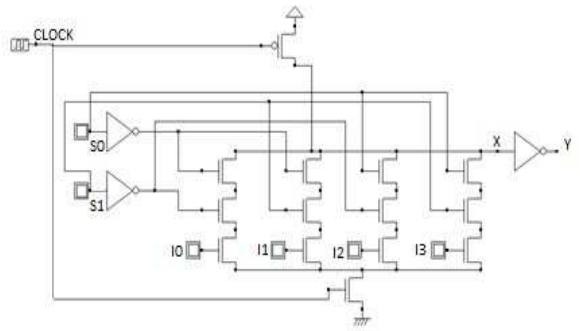


Figure3: a) Domino Logic



b) Multiplexer using domino logic

IV. DESIGNING 4:1 MULTIPLEXER USING KEEPER TECHNIQUE

The weak keeper circuit is a circuit that fixes the input level to the high level or the low level even when the I/O pins are not driven from the outside. The keeper transistor supplies a small amount of current from the power supply system to the dynamic node of a gate so that the charge put away in the dynamic node is maintained. The weak transistor is used in the domino logic in order to increase the noise immunity and reduction of leakage current.

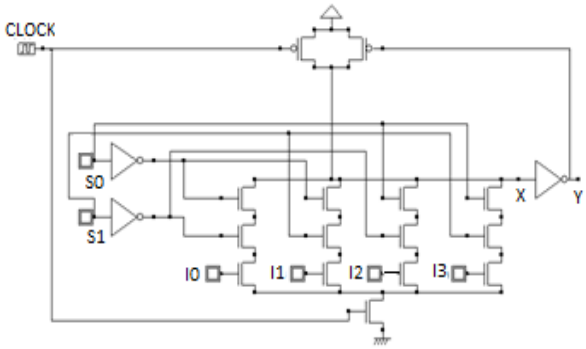


Figure 4: MUX using keeper technique

Whenever the input X is high, the ouput Y is low and keeper is on to prevent the input from floating and during this precharge state the capacitor is charged. When the input X is low, the keeper at first restricts the transition because it must be much weaker than the pull down network. Finally, the output rises, then the keeper is off in order to avoid the static power consumption. The 4:1Multiplexer utilizing conventional week fixed keeper logic technique is appeared in Figure 4.

V. DESIGNING OF MULTIPLEXER USING INVERTER FEEDBACK TECHNIQUE

In inverter feedback technique, the feedback signal is generated by connecting the output of a week CMOS inverter to the gate of the PMOS keeper transistor instead of directly connecting the gate output to the gate of PMOS keeper. The 4:1 Multiplexer using the inverter feedback technique is shown in Figure 5. Here, the feedback keeper transistor is independent on the output load. So the inverter feedback is optimizing freely without concerned about the gate output terminals connected together (diode footer) is connected in series with the pull-down. The 4:1 Multiplexer using inverter feedback is shown in the figure 6.

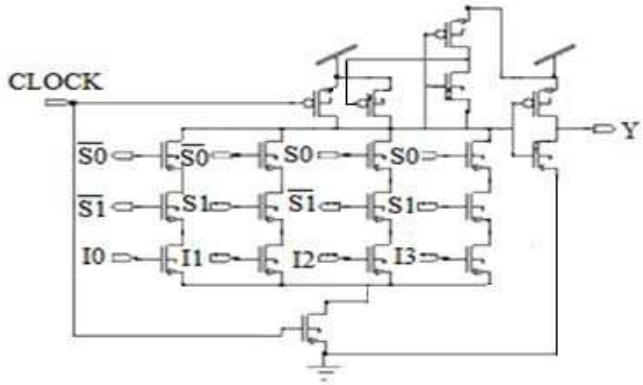


Figure 6: MUX using inverter feedback logic

VI. SIMULATION RESULTS

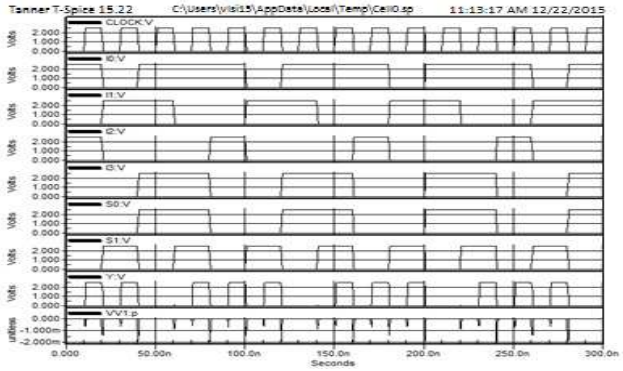


Figure7: Simulation output Pattern of the 4:1 Multiplexer Design using the Inverter Feedback.

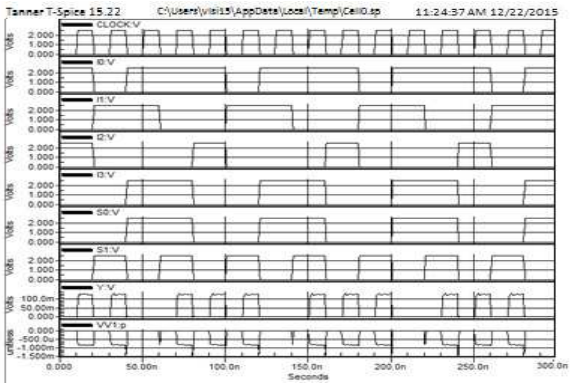


Figure8: Simulation output Pattern of the 4:1 Multiplexer Design using Conventional keeper technique

A. ANALYSIS

Parameters	Conventional Weak Fixed Keeper	Inverter Feedback
Power Consumption (mW)	0.32	0.061
Number of transistor	23	21
Propagation Delay (n-sec)	10.9	10.2
Power Delay Product (m-nJ)	3.41	0.64

B. Abbreviations and Acronyms

MUX- Multiplexer

VII. Conclusion

In this paper, the multiplexer was designed using different domino logic design techniques where the power, delay and area are reduced. Based on the simulation results, we can conclude that the inverted feedback technique performs tremendously well than other logic techniques.

REFERENCES

[1] Y.Varthamananand.Kannan,"PerformanceEvaluationofReversibleLogicBasedCNTFETDeMultiplexer", *International Journal of Electrical Engineering and Technology* (IJEET), 4(3), 2013, pp.53–62.

[2] Dadoria AK, Panwar U. Comparison on different domino logic design for high- performance and leakage-tolerant wide OR gate. International Journal of Engineering Research and Applications. 2013.

[3] FarshadMoradi, TuanVuCao, ElenaI. Vatajelu, AliPeiravi, Hamid Mahmoodi, DagT.Wisland,"Domino logic designs for high-performance and leakage-tolerant applications,"

[4] SauvagyaRanjanSahoo, Kamala KantaMahapatra," Performance Analysis of Modified Feedthrough Logic for Low Power and High Speed", IEEE-International Conference on Advances in Engineering, Science And Management (ICAESM -2012) March 30, 31, 2012.

[5] Salendra.Govindarajulu, Dr. T.Jayachandra Prasad, "Design of High Performance Dynamic CMOS Circuits in Deep Submicron Technology", SalendraGovindarajuluet. al. / International Journal of Engineering Science and Technology Vol. 2(7), 2010.

[6] R. G. D. Jeyasingh and N. Bhat, "A lowpower, process invariant keeper design for high speed dynamic logic circuits," in Proc. ISCAS, 2008, pp. 1668–1671.

[7] Chua-Chin Wang, Chi-Chun Huang, Ching-Li Lee, and Tsai-Wen Cheng, " A Low Power High-Speed 8-Bit Pipelining CLA Design Using Dual-Threshold Voltage Domino Logic" ,In *IEEE Transactions on very Large Scale Integration (VLSI) Systems*, Volume 16, No. 5, May 2008.

[8] M. Anis, M. Allam, and M. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 2, pp.71–78, Apr. 2002. Y. Lih, N. Tzartzanis, and W. W. Walker, "A leakage current replica keeper for dynamic circuits," IEEE J. Solid-State Circuits, vol. 42, no.1, pp. 48–55, Jan. 2007.

[9] H. Kim, K. Roy, S. Hsu, R. Krishnamurthy, and S. Borkar, "A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 6, pp. 646–649, Jun. 2006.

[10] S. M. Kang, Y. Leblebici, 'CMOS Digital Integrated Circuits: Analysis & Design', TATA McGraw- Hill Publication, 3e, 2003.

[11] Hamid Mahmoodi-Meimand and KaushikRoy, "Diode-Footed Domino: A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style,"*IEEETransactionsonCircuitsand Systems-1*, vol. 51,no. 3, pp 495-503, March. 2004.

[12] L. Ding and P. Mazumder, "On circuit techniques to improve noise immunity of CMOS dynamic logic," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 9, pp. 910–925, Sep. 2004.

[13] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicron CMOS circuits,"*Proc. IEEE*, vol.91, pp. 305–327, Feb. 2003.

[14] M. H. Anis, M. W. Allam, and M. I. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," *IEEE Trans. Very Large Scale (VLSI) Syst.*, 2002.

[15] Mohamed Elgebaly and ManojSachdev, " A leakage Tolerant Energy Efficient Wide Domino Circuit Technique " 2002 IEEE.

[16] J.M. Rabey, A. Chandrasekaran and B. Nicolic, Digital Integrated Circuits:Design Perspective, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2000.

[17] John P. Uyemura, "CMOS Logic Circuit Design", Springer, 1999.

[18] L.T. Clarke, G. F. Taylor, "High fan-in circuit design," *IEEE Journal of Solid-State Circuits, vol. 31*, Issue 1, January 1996, pp.91-96.