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DESIGN AND SIMULATION OF TRANSISTOR CLAMPED H-BRIDGE BASED CASCADED MULTILEVEL INVERTER USING MCPWM TECHNIQUE

SINDHOOJA H P [#1] and BALAJI CHAKRAVARTHY P [*2]

[#] *M tech in Power Electronics, Department of Electrical and Electronics Engineering, RNSIT, Bengaluru, India.*

[*] *Asst. Professor, Department of Electrical and Electronics, RNSIT, Bengaluru, India.*

***Abstract*— Multilevel converters offer high power capability, resulting with lower output harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. This paper presents a new topology of the multilevel inverter with feature like output voltage boosting capability along with capacitor voltage balancing .The proposed multilevel inverter uses conventional transistor clamped H-bridge (TCHB) with an bidirectional switch and four auxillary switches producing a boost output voltage . The single unit of new topology produces five-level output with output voltage double the input DC voltage where as a single unit of conventional H-bridge produces three-level ouput voltage similar to input DC voltage. This control scheme can also be used for the charge balance control with multiple input DC sources in any given topology. The proposed multilevel inverter topology is modelled using matlab/simulink. From the results the proposed inverter provides more output voltage.**

***Index Terms*— TCHB,MCPWM**

I. INTRODUCTION

With the more utilization of renewable energy, especially grid-tied photovoltaic's, the requirement to have a superior gradesingle-phase inverter has more important. The traditional technology used for single phase inverters usually consists of square-wave or pwm inverters. The square wave type is the easy method to generate AC from DC; still it be affected against low frequency pitch which makes complication in filtering of noise to prohibit these harmonics to return back to the primary side of the transformer. The pwm inverter, on another side, forces the harmonics to way up greater than the fundamental line frequency; thus, alleviate up the filtering necessity of the inverter. However, the most failing of pwm inverter is the enlarged switching failure due to the repeated switching behavior of the electronic switches inside the inverter.

The function of the inverter is to change DC to AC power. Inverters are fundamental part of certain technologies containing continuous power supplies, induction heating, high-voltage direct current power transmission, variable frequency drives, electric vehicle drives, and multiple renewable energy applications. These technologies use inverters to accomplish particular goals, but all of these produce AC from a DC input.

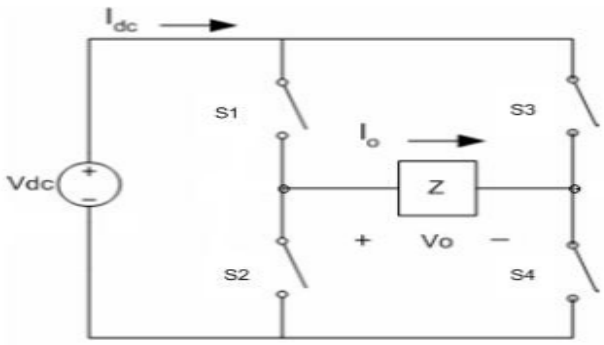


Fig .1.1 H-Bridge Single-Phase Inverter.

Multilevel inverter (MLI) is divided into three types; they are neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). For a higher number of output levels (>5), NPC and FC require complicated techniques for maintaining its capacitor voltage in the balanced state while CHB needs a more number of isolated DC sources. Aside from the above defects, MLIs needs more number of semiconductor devices which raises its cost and reduction in the reliability.

According to a newly conducted industry-based study on power converters, the semiconductor devices are the utmost sensitive parts which show low reliability of MLI as in comparison with two-level inverters. Hence, fault tolerance is one of the major concerns in many industrial applications where continuity is utmost important, such as wind turbines and PV cells. Fault tolerance in MLIs is achieved by adding redundant states along with thesuitable reconfiguration of control strategy under faulty condition. Redundancy can only be accomplished by adding some devices in series/parallel in the conventional topologies. Hence,certain modifications in conventional topologies are done in order to operate MLIs in fault scenarios.

A three cell four-level FC topology with one switch fault tolerant capability on each of its legs. Fault tolerance is achieved by shorting the faulted switch and reconfiguring the control strategy. This topology uses additional SCR with each IGBT and pair of bidirectional switches in each leg which increases its cost. Topologies of propose somemodified topologies of NPC with two types of fault tolerant features,

i.e. partial fault solution and complete fault solution. In partial fault solution, some levels are lost after the fault is reconfigured whereas in complete fault solution number of output levels is same after fault reconfiguration as in normal state. In all the modified topologies, the fourth leg of FC is added, which helps to keep the neutral point voltage oscillation as low as possible. The drawback of this topology is the inability to tolerate faults on its inner leg switch and proposes fast fault detection technique for CHB based on output voltage, frequency analysis; the fault is detected using an improved threshold level due to which faulty conditions and transient conditions are easily discriminated, but it cannot detect some open circuit faults which are its limitation.

Five-level transistor clamped H-bridge (TCHB) inverter which can be generalized for any number of levels by using cascading connections. TCHB inverter for symmetrical configuration was first proposed. It reduces the number of switches and DC sources as compared with CHB and also does not require any complicated circuits for maintaining its capacitor voltage in the balanced state.

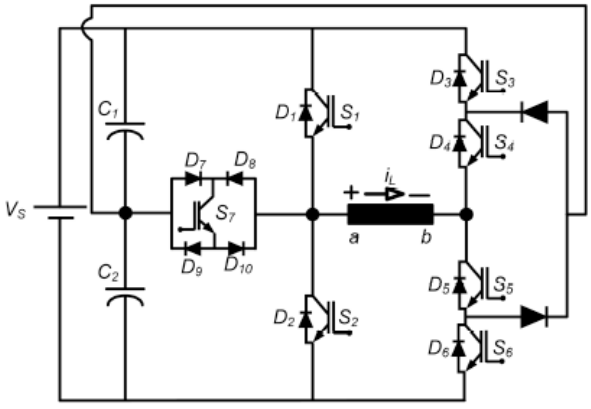


Fig.1.2 Modified five-level transistor clamped H-bridge inverter

Fig. 1.3 suggests one phase of the Cascaded H-Bridge multilevel converter with N H-Bridges related in series. The output section voltage of 2N+1 levels will be acquired from this converter.

One of the principle disadvantages of the Cascaded H-Bridge converter is the voltage unbalance that would appear on the DC side of the exceptional H-Bridges. In order to avoid those voltage unbalances, an good enough manage approach have to attain the energetic electricity absorbed with the aid of each H-Bridge to be same to the power losses present in the H-Bridge. Therefore an adequate managemethod of the Cascaded H-Bridge converter primarily based STATCOM have to regulate the active powermanaged through every H-Bridge for my part. But it must beguaranteed that the reactive power introduced by using all the H-Bridges is equitably distributed.

In the bibliography numerous Cascaded H-Bridge multilevel converter programs are provided. In maximum of them theconverter is used as an inverter providing energy to an industrial force. In such packages an unbiased electricity supply is required for each DC bus. In this form ofapplications the voltage unbalance problem isn't always gift, however the energetic power provided through every bridge must be controlled so as to minimize the voltage ripple of the DCBus capacitor [5, 6]. In [7] a compilation of DC-hyperlink voltageripple minimization control strategies is presented.

There also are several references where the Cascaded HBridge topology is used for reactive-energy repayment packages. Classically low frequency modulation techniques had been used due to the restrictions of the high-power digital switches. The commutation frequency became equal or very just like the line frequency [8-12].

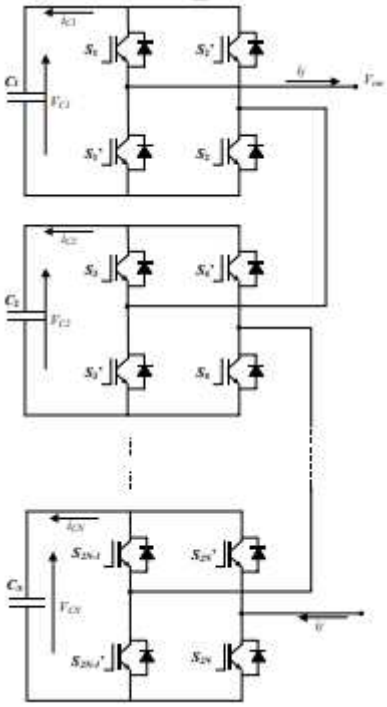


Fig.1.3 single phase cascaded N-level H-bridge inverter

The manipulate method provided in [17] permits the DC-Bus voltage balancing law, and the reactive power of the H-Bridges are controlled as properly. But the proposed set of rules is based totally in a simplified converter model, and on this version the 3 H-Bridges positioned on the identical stage in the 3 stages are grouped and dealt with as an man or woman H-Bridge.

This makes a speciality of the cascaded multilevel inverter topology. Generally, among the three topologies, the cascaded multilevel inverter has the ability to be the maximum dependable and reap the excellent fault tolerance owing to its modularity; a function that allows the inverter to maintain running at lower strength stages after cellular failure [29]-[31]. Modularity alsolets in the cascaded multilevel inverter to be stacked without difficulty or high electricity and excessive voltage packages. The cascaded multilevel inverter commonly accommodates several identical unmarried segment H-bridge cells cascaded in series at its output facet. This configuration is normally called a cascaded H-bridge (CHB), which can be categorised as symmetrical if the dc bus voltages are equal in all of the series energy cells, or as asymmetrical if otherwise. In an asymmetrical CHB, dc voltages are numerous to supply extra output degrees [2], [32]. Consequently, inverter layout becomes more complex as each electricity cell has to be sized for that reason to the unique power ranges, which include isolated dc assets. This makessymmetrical CHB modularity wonderful over

asymmetrical with regards to renovation and value.

II. Procedures For Paper Submission

The circuit topology for the proposed system is shown below:

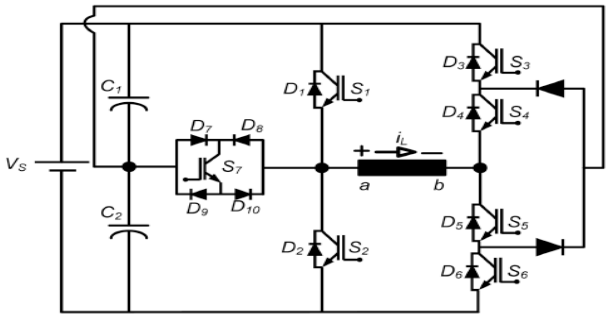


Fig.2.1Modified five-level transistor clamped H-bridge inverter.

The above configuration represents the five level H-bridge inverter. It consists of single DC source which is used to power the inverter. The H-bridge inverter has a two leg configurations: leg one consists of two IGBTs switch S1 and S2. Leg two has a neutral point clamped switch configuration which consists of four IGBT switch S3,S4,S5 and S6.Between the switches clamping diodes are connected. These diodes are used to clamp the blocking voltage of the switch.One bidirectional IGBT switch is connected across the DC voltage source. The two series connected capacitor having equal capacitance value and get charged to half of the DC supply voltage.During the normal operation, the inverter have capability of producing five level output. Five level outputs are: Vs/2, Vs, 0, -Vs, -Vs/2.

A. Fault tolerant strategies

Fault tolerant strategy includes three main categories:

1. Fault on switches S1 and S2.
2. Fault on switches S3 and S6.
3. Fault on capacitors C1 and C2.

B. Fault on switches S1 and S2:

When fault occurs on switch S1, the voltage across the capacitor C1 decreases and voltage across the capacitor C2 increases slightly.When fault occurs on the switch S2, voltage across the capacitor C1 increases and voltage across the capacitor C2 decrease slightly. Even fault occurs on S1 and S2, the inverter gives three level outputs: Vs/2, 0 and –Vs/2. When fault is cleared, the voltage across the capacitor is half of DC source voltage.

III. Modulation Strategy

The gate pulses for the IGBT switches are feed by using the use of multi-carrier pulse width modulation technique. Here four carrier waves whose frequency 5kHz, that is as compared with single sinusoidal reference sign having a frequency of 50Hz. For ordinary operating situations, modulation index is cohesion. For fault situation it will become 1/2.

Under fault situations of leg one and leg , modulation index fee is 0.5 and switchin method is equal as everyday condition. Under the fault on capacitor, modulation approach is equal as regular circumstance.

IV. Simulation of the Proposed Topology

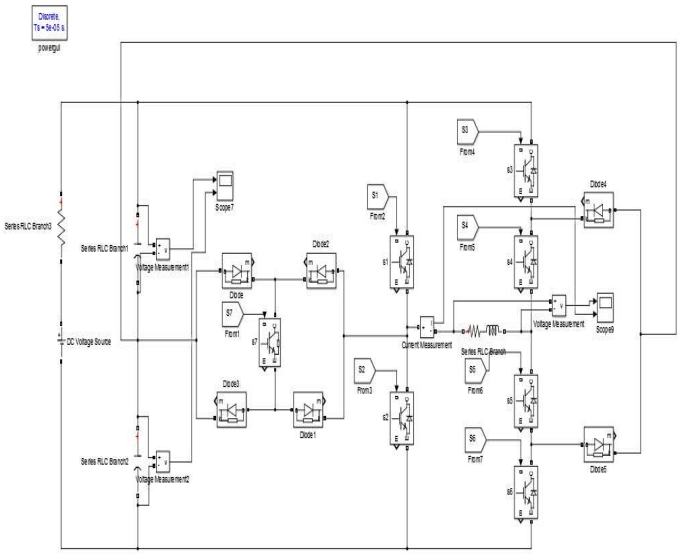


Fig.4.1 Simulation circuit of five-level transistor clamped H-bridge inverter.

The simulation circuit consists of two scopes. Scope1 shows the waveform of voltage and current across the load of the inverter. Scope2 shows the waveform of voltage across the two capacitors. Internal resistor is connected in series with DC source having small resistance value of 0.001Ω.

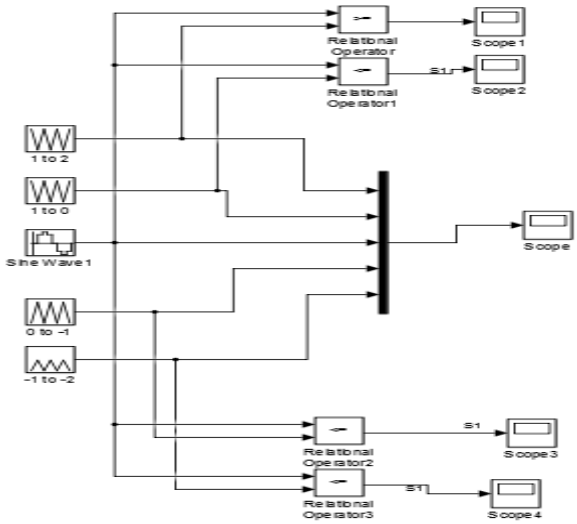


Fig.4.2Modulation strategy

The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency wm and amplitude Am. At every instant each carrier is compared with the modulating signal. Each comparison gives 1 (-1) if the modulating sinusoid is greater than (lower than) the triangular carrier in the first (second) half of the fundamental period, 0 otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Obviously, the actual driving signals for the power devices depend on the particular structure chosen to realize the inverter and thus can be derived from the results of the modulating-carriers comparison by means of a simple logic

circuit. In the case of three-phase inverters we can choose between two different ways in which the switching waveforms of the three legs are produced. To comply with the requirements for a threephase system, we need always three 120” phase-shifted modulating sinusoids. The two possibilities are distinguished by the use of the carrier signals. First, a single carrier set may be used to be compared with the three modulating sinusoids (single-phase modulation). Second, three different carrier sets with 120” phase displacement among themselves may be used, each to be compared with the corresponding sinusoid (three phase modulation).

V. HARDWARE IMPLEMENTATION

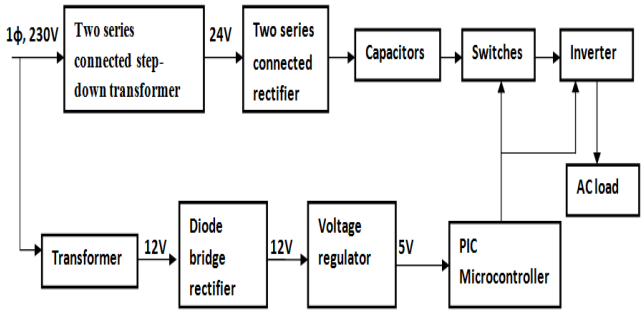


Fig.5.1:Block diagram for hardware model

Explanation of hardware model:

At the input side, single phase 230V AC supply is given to two step-down transformers, which are connected in series. Each transformer provides 24V AC output. Totally 48V AC input.

Each transformer output is given to the diode bridge rectifier which converts AC into DC. The output of the two diode bridge rectifier is 48V. This rectifier supply charges the two capacitors to half of the DC supply voltage (24V).

By using seven transformers, whose input voltage is 230V AC gives step-down output is about 12V. the 12V output of transformer given to the diode bridge rectifier. It gives 12V DC. The output of rectifier is given to the voltage regulator (LM7805). Voltage regulator which provides a 5V regulated output from the 12V unregulated input.

The regulated output of LM7805 is input to the microcontroller (PIC16F72) 28 pin. This provides a gate pulses to the switches present in the inverter.

The AC load (bulb) is connected across the inverter. The fault conditions of switches are obtained by disconnecting the gate pulses for the corresponding switch.

During the normal operation condition, gate pulses are provided for all seven switches. Connect CRO probes across the probes. Five level output voltage are observed in CRO. Multimeter shows 48V and 2.2 Amps.

During faulty operating conditions, disconnect the gate pulses of corresponding switches. At that time, voltage across the load is 28V and current is 0.6 Amps. Output voltage and current is reduced in Faulty state.

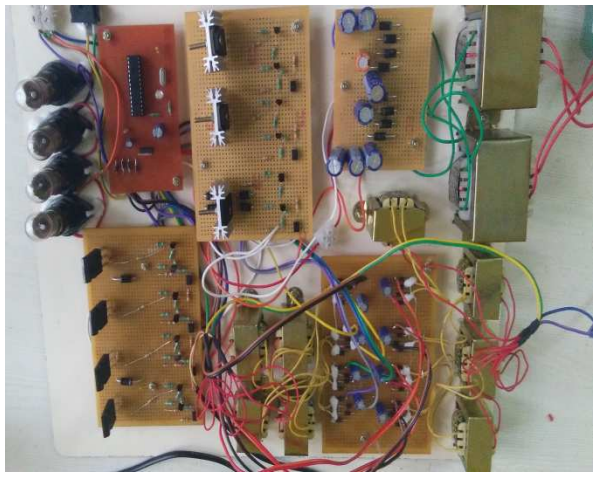
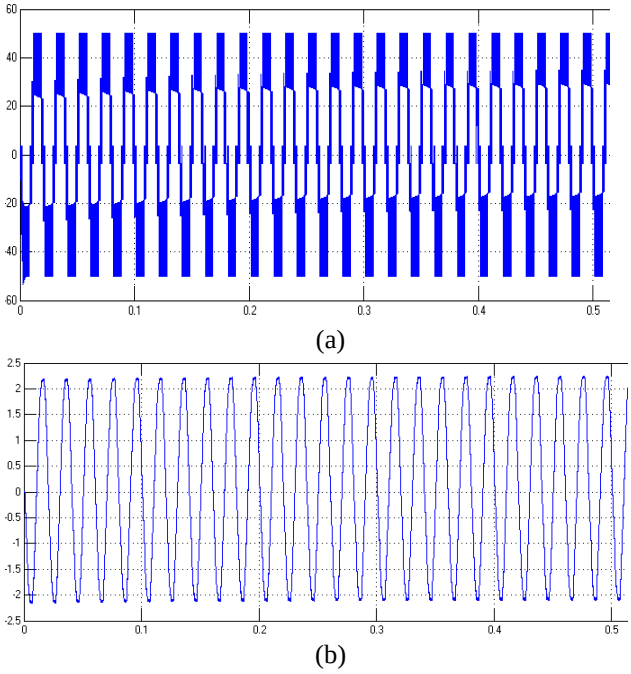


Fig 5.2 Prototype of proposed system.

VI. RESULTS

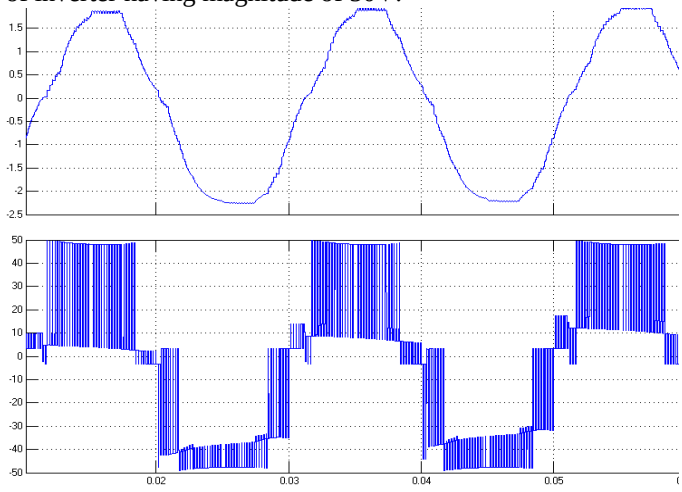


(a)

(b)

Fig 6.1 waveform of voltage and current across the inverter under normal operation.

The above figure represents the five levelvoltage waveform of inverter having magnitude of 50V.



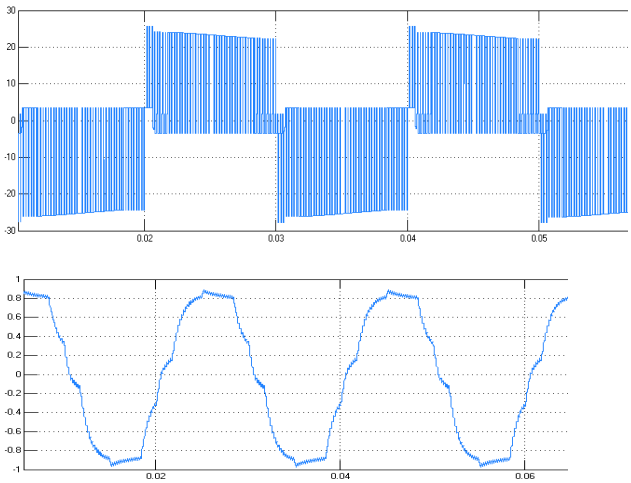


Fig.6.2 (a) waveform of voltage under fault on switch S3 and S6. (b) Waveform of current under fault on switch S3 and S6.

Experimental results

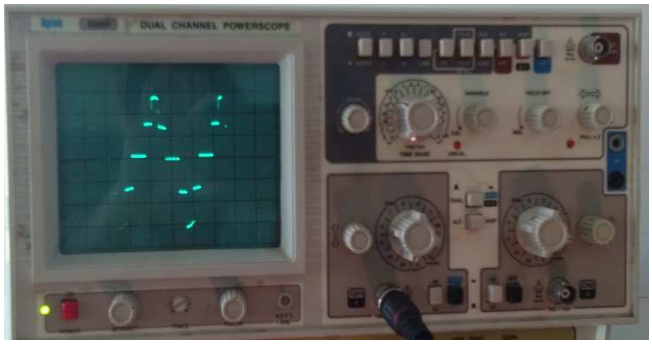


Fig.6.3 Experimental waveform during normal operation of inverter.

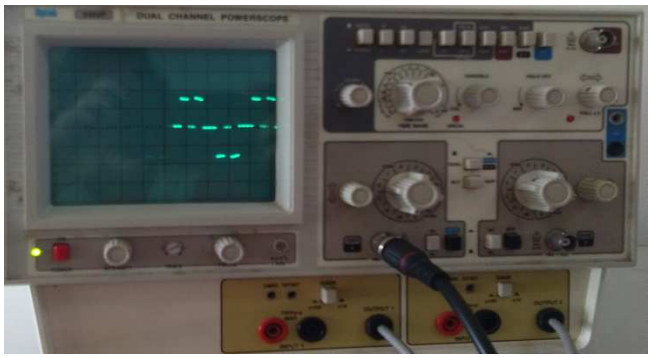


Fig.6.4 Experimental waveform during switching fault of inverter.

VII. Conclusion

The development in reliability of TCHB inverter is performed by means of including one NPC leg in location of CHB leg. This NPC leg facilitates in creating internal voltage redundancies because of which inverter can nonetheless be operated underneath faulty conditions as 3-degree inverter with the aid of reconfiguring the manage technique. Moreover, fault on the capacitor can be tolerated, however with multiplied voltage ripples within the capacitor voltage below faulty conditions. Proposed topology poses upload on gain of self-voltage balancing of its capacitor voltage each underneath normal and post-fault state.

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