Reversible Logic Gates: Less Dissipation Of Heat And Low Power Consumption

M.VENKATESWARA RAO^{*1} and D.DAYAKAR RAO^{#2}

*Student, Dept of Electronics and Communication, Sree Vahini Institute of Science and Technology, Tiruvuru., A.P, India [#]Asst Professor, Dept of Electronics and Communication, Sree Vahini Institute of Science and Technology, Tiruvuru., A.P., India ¹tallurianusha7@gmail.com

²dasuji12@gmail.com

Abstract— In this technological world development in the field of nanometer technology leads to minimize the power consumption of logic circuits. Reversible logic design has been one of the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. In digital systems code conversion is a widely used process for reasons such as enhancing security of data, reducing the complexity of arithmetic operations and thereby reducing the hardware required, dropping the level of switching activity leading to more speed of operation and power saving etc. This paper proposes novel Reversible logic design for code conversion such as Binary to Gray code, Gray to Binary code, BCD to Excess 3 code, Excess 3 to BCD code.

Keywords: Reversible logic gates, reversible code converter, quantum computing, VLSI.

I. INTRODUCTION

One of the major goals in modern circuit design is reduction of power consumption. As demonstrated by R.Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss [1]. Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Hence,. In 1973, Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs [4-6]. This paper presents design of reversible code converters includes reversible binary to gray code converter, reversible gray to binary converter, reversible BCD to excess 3 code converter, reversible excess3 to BCD code converter. The paper is organized as follows section II presents the literature survey on reversible logic gates, section III presents the design of proposed reversible code converters circuits, section IV presents the analysis of the proposed methods, section V presents the conclusion and future work.

II. LITRETURE SURVEY

This section introduces the basics of reversible logic gates and various reversible logic gate proposed. Reversible logic has received significant attention in recent years. It has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology. It is not possible to construct quantum circuits without reversible logic gates. Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits because in a reversible logic circuit, we are not allowed to use fan-out and feedback [4]. The performance of the reversible circuit based on the following parameters

1. Garbage output: The number of unused outputs present in the reversible logic circuit

2. Number of reversible logic gates: Total number of reversible logic gates used in the circuit.

3. Delay: Maximum number of unit delay gates in the path of propagation of inputs to outputs.

4. Constant inputs: The number of input which are maintained constant at 0 or 1 in order to get the required function.

The different types reversible logic gates available is listed below

Reversible logic gates: An nxn reversible gate can be represented as[8]:

IV = (A, B, C,)

OV = (P,Q,R,....)

Where IV and OV are input and output vectors respectively.

International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE) ISSN: 0976-1353 Volume 11 Issue 6 –NOVEMBER 2014.

Gate	Diagrammatic representation	Inputs	Outputs
Feynman gate	$\begin{array}{c} A \\ B \end{array} FG P = A \\ Q = A \oplus B \end{array}$	Α,Β	$P \cdot Q$ P = A $Q = A \bigoplus_B$
Toffoli gate	$\begin{array}{c} A & & & \\ B & & \\ C & & \\ \end{array} \begin{array}{c} TG & & \\ P = A \\ Q = B \\ R = AB \oplus C \end{array}$	A, B, C	P,Q,R P = A Q = B $R = AB \bigoplus C$
Fredkin gate	$A \longrightarrow P = A$ $B \longrightarrow FRG \qquad Q = A'B \oplus AC$ $C \longrightarrow R = A'C \oplus AB$	A, B, C	P,Q,R P = A $Q = A \cdot B \bigoplus A C$ $R = A \cdot C \bigoplus A B$
Peres gate	$\begin{array}{c} A \\ B \\ C \end{array} \begin{array}{c} P G \\ P G \\ C \end{array} \begin{array}{c} P = A \\ Q = A \oplus B \\ R = AB \oplus C \end{array}$	A , B , C	P,Q,R P=A $Q=A \bigoplus B$ $R=AB \bigoplus C$
URG gate	$\begin{array}{c} A \\ B \\ C \end{array} \qquad \begin{array}{c} P = C \oplus AB \\ Q = B \\ R = C \oplus (A + B) \end{array}$	A , B , C	P,Q,R $P = C \bigoplus_{AB}$ Q = B $R = C \bigoplus_{(A+B)}$
HNG gate	A $P = A$ B $Q = B$ C $B = A \oplus B \oplus C$ D $S = (A \oplus B)C \oplus AB \oplus D$	A.B.C,D	P.Q.R.S P = A Q = B $R = A \bigoplus B \bigoplus C$ $S = (A \bigoplus B)C \bigoplus B \bigoplus$

TABLE 1 EXISTING REVERSIBLE LOGIC GATES

III. PROPOSED REVERSIBLE CODE CONVERTERS

Designing of reversible logic circuit is challenging task, since not enough number of gates are available for design. Reversible processor design needs its building blocks should be reversible in this view the designing of reversible

code converters became essential one. In the digital domain, data or information is represented by a combination of 0's and 1's. A code is basically the pattern of these 0's and 1's used to represent the data. Code converters are a

class of combinational digital circuits that are used to convert one type of code in to another. Some of the most prominently used codes in digital systems are Natural Binary Sequence, Binary Coded Decimal, Excess-3 Code, Gray Code, ASCII Code etc. Like any combinational digital circuit, a code converter can be implemented by using a circuitry of AND, OR and NOT gates. Here this paper focuses more on conversion of code between binary to gray and BCD to excess-3.

3.1 Reversible Binary to Gray and Gray to binary code converter

Binary to Gray code converters used to reduce switching activity by achieving single bit transition between logical sequences. If Input vector is I(D,C,B,A) then the output vector o(Z,Y,X,W). The circuit is constructed with the help of Feynman Gate (FG) gate[7], the Table 3.1 shows the truth table of FG gate and figure 3.1 & 3.2 shows the circuit diagram of reversible Binary to Gray code converter & Gray to Binary code converter.

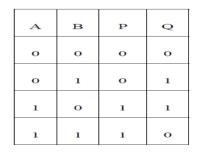


TABLE 3.1 : TRUTH TABLE OF FG GATE

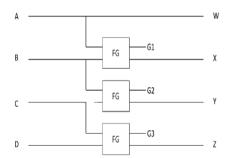


Figure 3.1 Circuit diagram of Reversible Binary to Gray code converter

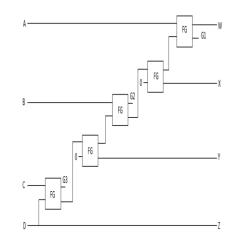


Figure 3.2 Circuit diagram of Reversible Gray to Binary converter

3.2 Reversible BCD to Excess-3 code and Excess-3 to BCD code converter

BCD to Excess-3 code converter used in arithmetic operational circuits to reduce the overall hardware complexity, The circuit is constructed with the help of two reversible gates Feynman Gate (FG) and Universal Reversible Gate (URG)[9]. The truth table of FG gate presented in session 3.1 and the truth table of URG gate presented in table 3.2 and the circuit diagram of Reversible BCD to Excess-3 and Excess-3 to BCD shown in figure 3.3 & 3.4 respectively.

International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE) ISSN: 0976-1353 Volume 11 Issue 6 –NOVEMBER 2014.

Α	В	С	Р	Q	R
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	0	1	0

TABLE 3.2 TRUTH TABLE OF URG GATE

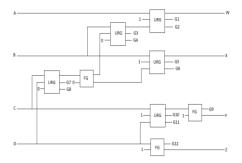


Figure 3.3 Circuit diagram of Reversible BCD to Excess-3 code converter

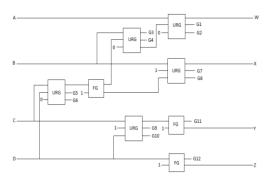


Figure 3.4 Circuit diagram of Reversible Excess-3 to BCD code converter

IV. RESULT AND ANALYSIS

The proposed reversible code converter is more efficient then the conventional code converters.

Evaluation of the proposed circuit can be comprehended easily with the help of the Table 3.3. the total logical operation involved in the proposed reversible code converter circuit is calculated with the help of following logical assignments

- a = XOR logic
- b = buffer
- c = NOT logic
- d = OR logic
- e = AND logic

for example if T = 2a+3d then the circuit involves 2numbers of XOR logical operation and 3 numbers of OR logical operations. The performance of the design is based on the number of gate, number of garbage (not used terminals) and number of constants, in this proposed design the above said parameters are optimized to greater extent.

Reversible Code Converters	No. of Gates	No. of Garbage	No. of Constants	Total logical calculation
Binary to Gray	3	3	Q	3a
Gray to Binary	5	3	2	3a+2b
BCD to Excess-3	8	12	8	3a+1b+2c+1d+1e
Excess-3 to BCD	8	12	8	2a+3c+1d+2e

TABLE 3.3 COMPARATIVE RESULT OF DIFFERENT REVERSIBLE LOGIC CIRCUITS

V. CONCLUSION

This paper has introduced and proposed reversible logic gates and reversible circuits for realizing different code converters like BCD to Excess-3, Excess-3 to BCD, Binary to Gray and Gray to Binary using reversible logic gates. The proposed design leads to the reduction of power consumption compared with conventional logic

circuits, the design proposed is implemented with FG and URG gates only in near future with the invent of new RLG the power consumption may reduced to little more greater extent, not only that there will be a chance of implementing different logic circuits using reversible logic gates and which intern helps to increase the energy efficiency to a greater extent.

REFERENCES

- Landauer, R., 1961. Irreversibility and heat generation in the computing process, IBM J.Research and Development, 5 (3): 183-191.
- [2] Bennett, C.H., 1973. Logical reversibility of computation, IBM J. Research and Development, 17: 525-532.
- [3] Kerntopf, P., M.A. Perkowski and M.H.A. Khan,2004. On universality of general reversible multiple valued logic gates, IEEE Proceeding ofthe 34th international symposium on multiple valued logic (ISMVL'04), pp: 68-73.
- [4] Perkowski, M., A. Al-Rabadi, P. Kerntopf, A.Buller, M. Chrzanowska-Jeske, A. Mishchenko, M.Azad Khan, A.Coppola, S. Yanushkevich, V.Shmerko and L. Jozwiak, 2001A general decomposition for reversible logic, Proc.RM'2001, Starkville, pp: 119-138.
- [5] Perkowski, M. and P. Kerntopf, 2001. Reversible Logic. Invited tutorial, Proc. EURO-MICRO, Sept 2001, Warsaw, Poland.
- [6] Thapliyal Himanshu, and M.B. Srinivas, 2005.Novel reversible TSG gate and its application for designing reversible carry look ahead adderand other adder architectures, Proceedings of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC 05). Lecture Notes of Computer Science, Springer-Verlag, 3740: 775-786.

International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE) ISSN: 0976-1353 Volume 11 Issue 6 –NOVEMBER 2014.

- [7] Feynman, R., 1985. Quantum mechanical computers, Optics News, 11: 11-20.
- [8] Saravanan. M., Cholan K., Abhishek G, 2010. Design of Noval Reversible Multiplier Using MKG Gate in Nanotechnology, Proceedings of National Conference on Automation Control and Computing (NCACC-10).
- [9] Mahammad, S.N., Veezhinathan, K. 2010. Constructing Online Testable Circuits Using Reversible Logic, IEEE Journal of Instrumentation and Measurement, Vol.59, No 1, pp. 101-109, Jan 2010
- 2010[10] Toffoli T., 1980. Reversible computing, Tech Memo MIT/LCS/TM-151. MIT Lab for Computer Science.
- [11] Peres, A., 1985. Reversible logic and quantum computers, Physical Review: A, 32 (6): 3266-3276.
- [12] Azad Khan, Md.M.H., 2002. Design of full adder with reversible gate. International Conference on Computer and Information Technology, Dhaka, Bangladesh, pp: 515-519.
- [13] Haghparast, M. and K. Navi, 2007. A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems. J. Applied Sci., 7 (24): 3995-4000.
- [14] Haghparast, M. and K. Navi, 2008. Design of a Novel Fault Tolerant Reversible Full Adder ForNanotechnology Based Systems, World Appl. Sci. J., 3 (1): 114-118.