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COMPARATIVE STUDY OF VARIOUS VLSI TECHNOLOGIES FOR GENERATING 16 BIT EVEN PARITY

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Abstract— **The primary objective of this paper is to do the comparative study of various techniques for generating and 16 bit even parity. The technique that is often used for error detection is parity, which refers to the number of bits that are 1 in a code word. Parity error detection involves increasing the code length by one bit, called the parity bit [6]. An even parity bit generator generates an output of 0 if the number of 1's in the input sequence is even and 1 if the number of 1's in the input sequence is odd. In terms of delay, transmission gate logic is best for design. In terms of power consumption, GDI logic is best for design. In terms of both, the delay and power consumption, GDI logic and pass transistor logic is best for design.**

***Keywords*—parity generator, xor gate, cmos, GDI.**

I. INTRODUCTION

The *parity* technique is used for error detection, which refers to the number of bits which are 1 in the code word. Parity error detection involves increasing the code length by one bit, called the *parity bit* [6]. An even parity bit generator generates an output of 0 if the number of 1's in the input sequence is even and 1 if the number of 1's in the input sequence is odd. For example, if the original code word is 1011, the augmented code word is 10111 [6]. The checker circuit gives an output of 0 if there is no error in the parity bit generated. Thus it basically checks to see if the parity bit generator is error free or not [6].

Recently, the success of optical devices such as semiconductor optical amplifiers (SOA) in all-optical signal processing and optical computing has triggered great research interest in them [1–3]. These devices have shown ability to perform direct bit-manipulation in the optical domain which may be used for address recognition, packet header modification and data integrity verification. For data integrity verification, an all-optical parity checker was proposed [4, 5]. As it is well known in electronic digital communication, parity check is one of the most widely used binary manipulations and is attached to a binary word before transmission of the data so that the receiver has the ability to verify the integrity of the recovered digital data. The optical parity checker can be generated by using an XOR gate and a single bit optical delay. Each bit in binary word is checked in order to generate the overall parity bit at end of the word.

Parity bit generator is used in digital communications where the messages are transmitted in the form of 1's and 0's. The message has to be transmitted between two points without any errors. By checking the message bits at the transmitter end and receiver end, it can be done easily. A parity bit is generated at the transmitting end and is transmitted along with the message bits through the transmission channel. The parity bit is generated again at the receiving end and is checked against the parity bit generated at the transmitter end. If both are same then message is error free otherwise message is different from the transmitted message. This method helps in detecting a one-bit error in message sequence but it doesn't correct the message sequence. This is the error detection methods used in digital communications.

II. BLOCK DIAGRAM

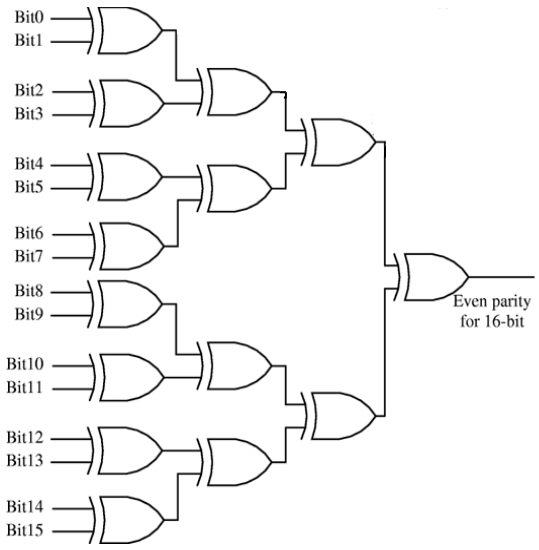

Fig 1: Even Parity Generator for 16 bits

III. VARIOUS TECHNOLOGIES

A. *Cmos Technology*

Complementary metal-oxide-semiconductor (CMOS) processes are popular for implementing integrated circuits. This is mainly due to low cost, but also because they enable the implementation of digital circuits with low power consumption. Complementary refers to the meaning that both NMOS and PMOS transistors are present. An NMOS transistor consists of heavily N-doped drain and source regions implanted in lightly P-doped. The drain and source is separated by a gate region.

CMOS is a technology for constructing integrated circuits, microprocessors, RAM and other digital circuits. CMOS technology is also used for image sensors, data converters etc used in types of communication. CMOS is also sometimes referred to as complementary-symmetry metal-oxide–semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistor (MOSFETs) for logic functions. Two characteristics of CMOS devices are high noise immunity and low static power consumption. Power is drawn when the transistors in the CMOS device are switching between on and off states. CMOS devices doesn't produce more heat like NMOS logic. CMOS allows high density of logic functions on the chip. This is the reason that CMOS became the most used technology in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field effect transistors, which has a metal gate electrode placed on the top of the oxide insulator, which in turn is on top of a semiconductor material. Metal Aluminium was used earlier but the material used presently is polysilicon. Other metal gates makes use of high-k dielectric materials in the CMOS process, as announced by Intel for the 45-nanometre node and beyond.

B. *Gate Diffusion Input (Gdi)*

Gate Diffusion Input (GDI) design technique was introduced as an alternative to CMOS Logic design. It was proposed for Silicon on Insulator (SOI) fabrication and twin-well CMOS processes. GDI technique allows implementation of logic functions using only two transistors. It is seen that area and dynamic power of combinatorial and sequential logic were significantly reduced by GDI technique, when compared to CMOS technique.

1) GDI CELL has three inputs: G - common gate input (of NMOS and PMOS), P- input for the source/drain of PMOS, and N - input for source/drain of NMOS).

2) The source of PMOS in a GDI cell is not connected to VDD and source of NMOS is not connected to GND . This feature gives GDI cell two extra input pins for use which makes GDI design more flexible.

3) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be easily biased with CMOS NOT gate.

C. *Pass Transistor Logic*

Pass transistor logic (PTL) gives many logic families used in design of many integrated circuits. It reduces the number of transistors used. It does this by eliminating unwanted transistors. Transistors are used as switches to pass logic levels between nodes of a circuit.[1] This decreases the number of active devices, but it has a disadvantage that the voltage difference between high and low logic levels reduces at each stage. Every transistor in series is less saturated at the output compared to its input.[2] If many devices are connected in series in a logic path, a gate may be required to get back the signal voltage to its full value. CMOS logic makes transistors ON so the output is connected to one of the power supply rails, so logic voltage levels in a sequential chain doesn't reduce. There is very less isolation between input signals and output signals, the designers take care the effects of un-intentional paths inside the circuit. For good operation, the design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided.[3] Simulation of circuits may be required to ensure adequate performance.

D. *Transmission Gate*

A transmission gate (analog switch), is an electronic element which selectively block or pass a signal level from the input side to the output side. This switch has a pMOS transistor and nMOS transistor. The gates are biased in a complementary fashion so that both the transistors are either ON or OFF. When the voltage on node D is a Logic 1, the Logic 0 is applied to node active-low D, allowing both transistors to conduct and pass the signal from IN to OUT. When the voltage on node active-low D is a Logic 0, the Logic 1 is applied to node D, turning both the transistors OFF and forcing a high-impedance condition on both the INPUT and OUTPUT nodes.

E. *Pseudo Nmos/Depletion Load Nmos*

D**epletion-load NMOS** is a technique of digital logic which uses only a single power supply voltage instead of more than one different power supply voltage. Although manufacturing integrated circuits required some additional processing steps, also the elimination of the extra power supply, and the improved switching speed. All this made this logic technique the good choice for many microprocessors and all other logic elements.

Depletion-mode n-type MOSFETs which are used as load transistors allow single voltage operation and they achieve a greater speed than possible with the pure enhancement-load devices. The depletion-mode MOSFETs are a better current source approximation than the simpler enhancement-mode transistors, when no extra voltage is available (this is one of the

reasons that early pMOS and nMOS chips demanded several voltages).

IV. Design Of Schematics Using Various Techniques

A. Design of Xor Gate Schematic Using CMOS Technology

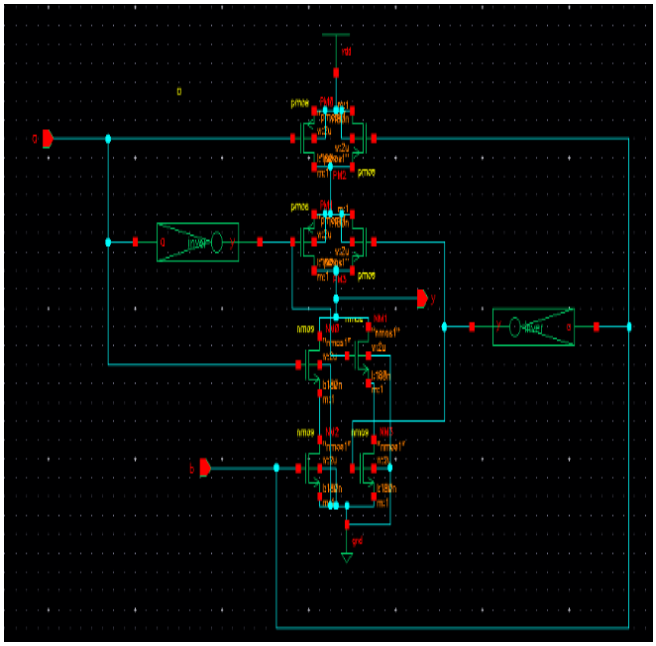

Figure 2: XOR Gate Schematic using CMOS Technology

B. Design of Even Parity Generator Schematic Using Cmos Technology

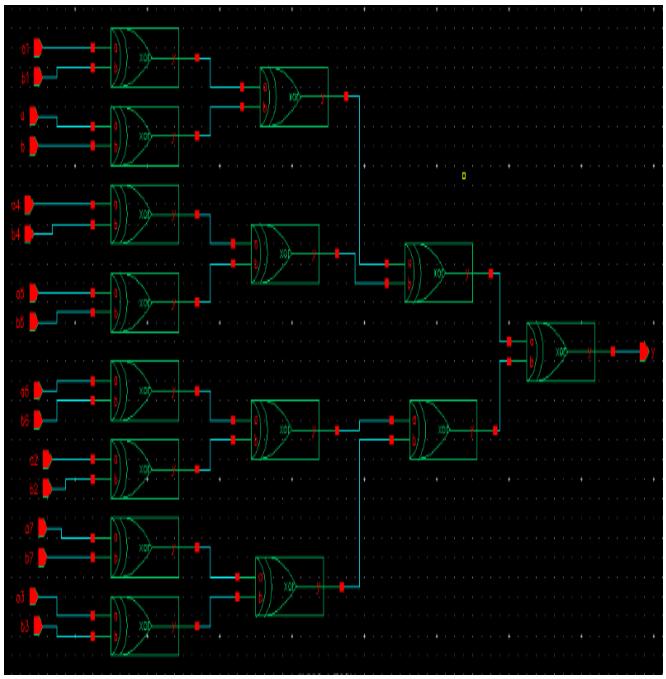

Figure 3 : Even Parity Generator Schematic using CMOS Technology

C. Design of Xor Gate Schematic Using Transmission Gate

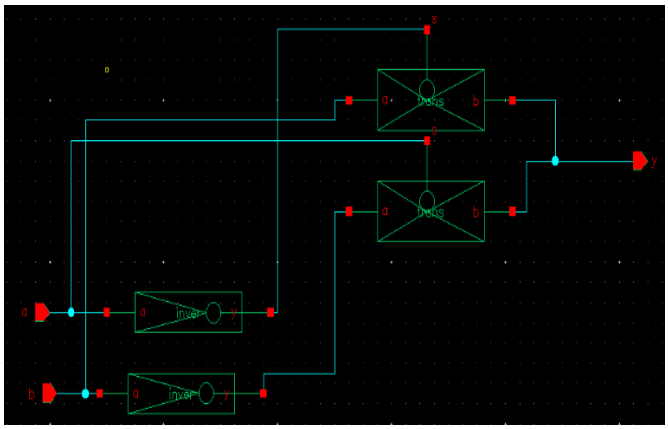

Figure 4: XOR Gate Schematic using Transmission Gate

D. Design of Even Parity Generator Schematic Using Transmission Gate

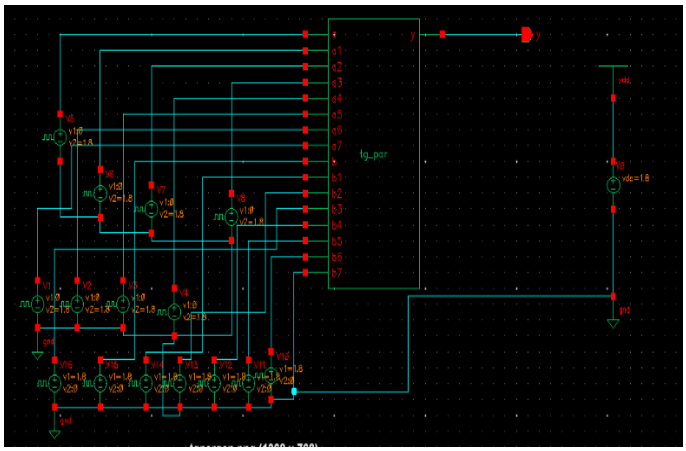

Figure 5: Even Parity Generator Schematic using Transmission Gate

E. Design of Xor Gate Schematic Using Gdi Technology

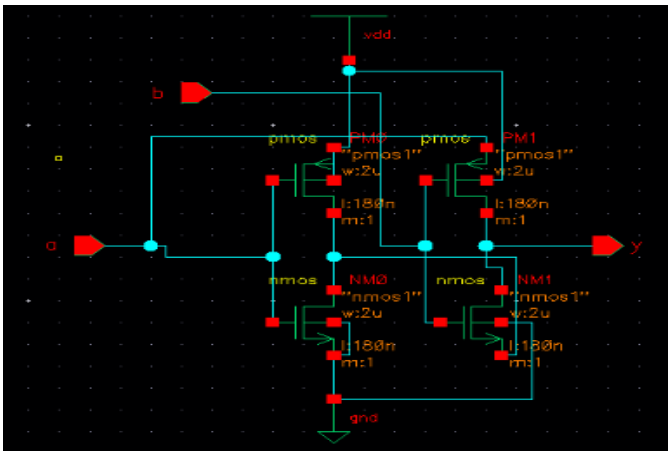

Figure 6: XOR Gate Schematic using GDI Technology

F. *Design of Even Parity Generator Schematic Using Gdi Technology*

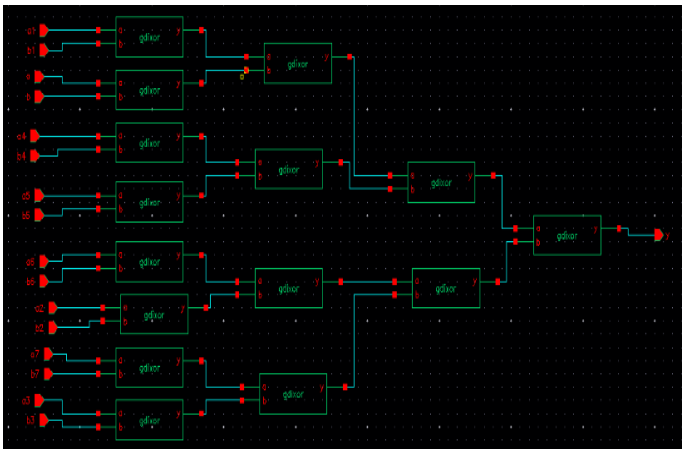

Figure 7: Even Parity Generator Schematic using GDI Technology

G. *Design of Xor Gate Schematic Using Saturated Load Technology*

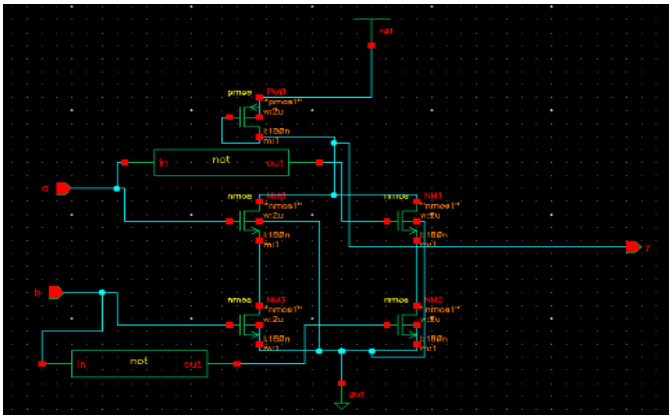

Figure 8: XOR Gate Schematic using Saturated Load Technology

H. *Design of Even Parity Generator Schematic Using Saturated Load Technology*

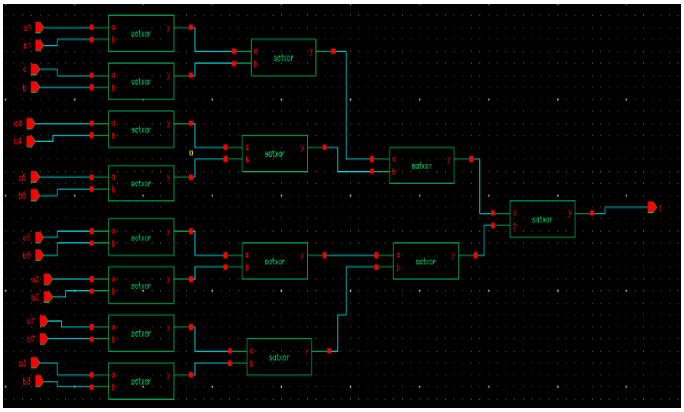

Figure 9: Even Parity Generator Schematic using Saturated Load Technology

I. *Design of Xor Gate Schematic Using Pass Transistor Logic*

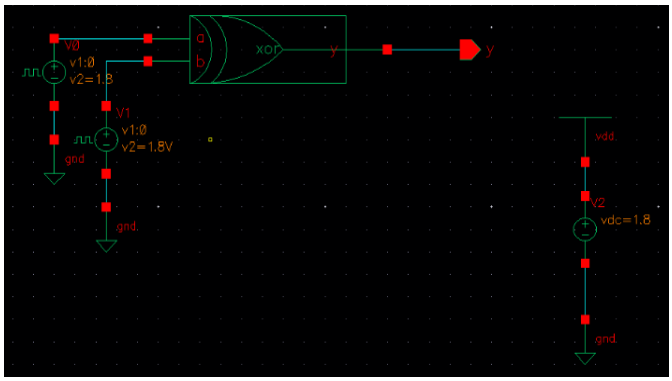

Figure 10: XOR Gate Schematic using Pass Transistor Logic

J. *Design of Even Parity Generator Schematic Using Pass Transistor Logic*

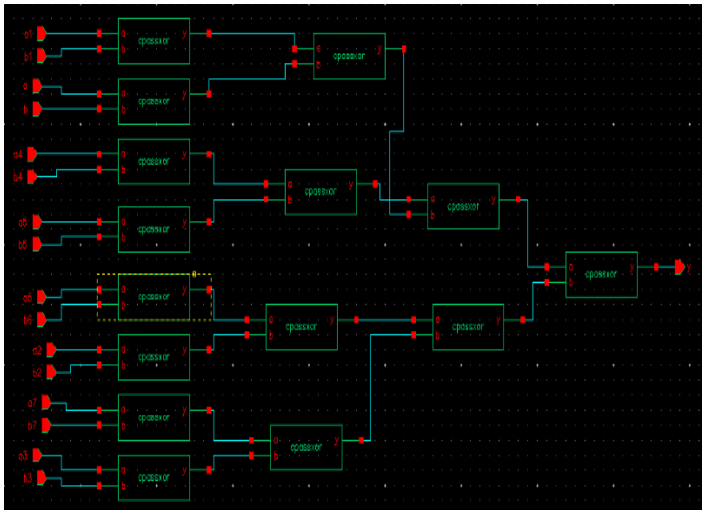

Figure 11: Even Parity Generator Schematic using Pass Transistor Logic

V. Simulation Results And Discussions

A. *Simulation Results of Xor Gate Schematic*

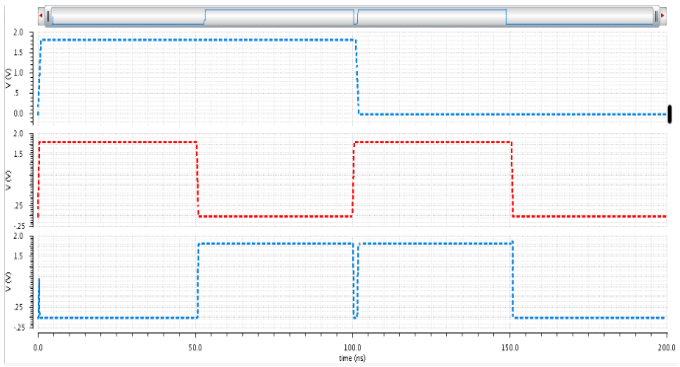

Figure 12: Results of XOR Gate using Pass Transistor Logic

B. Simulation Results of Even Parity Generator

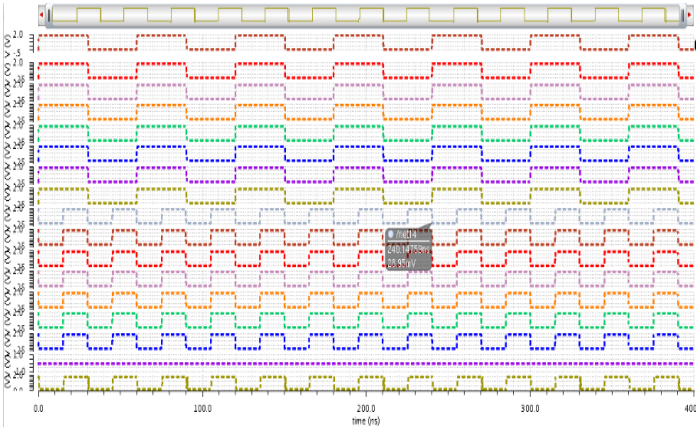

Figure 13: Results of Even Parity Generator using Saturated load and pseudo nmos logic

C. Comparison of Various Techniques for Design of Even Parity Generator

Technology	Delay (µs)	Power Consumption(mW)
CMOS	2552.31	16.587
TRANSMISSION GATE	172.35	11.318
PASS TRANSISTOR LOGIC	728.70	3.754
SATURATED LOAD	1854.94	2.619
PSEUDO NMOS	1852.48	3.122
GDI	755.26	0.151

VI. CONCLUSIONS

In terms of delay, transmission gate logic, GDI, pass transistor logic is best for design. In terms of delay, CMOS logic is worst for design. In terms of power consumption, GDI logic is best for design. In terms of power consumption, CMOS logic is worst for design. In terms of both, the delay and power consumption, GDI logic, transmission gate logic and pass transistor logic is best for design.

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