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AN IMPLEMENTATION OF AREA EFFICIENT & FAST ADDITION AND MULTIPLICATION OPERATION USING RADIX BASED MODIFIED BOOTH RECODING TECHNIQUE

Dr.T.Lalith Kumar[1], N.Shehanaz[2]

M.Tech, Ph.D, Associate Professor, Department of Electronics and Communication Engineering, Annamacharya Institute of Technology & Sciences, C.K Dinne, Kadapa-516003, India.
PG Student, Department of Electronics and Communication Engineering, Annamacharya Institute of Technology & Sciences, C.K Dinne, Kadapa-516003, India.

***Abstract* – It represents an area efficient design and Fast Addition & Multiplication operation using Radix based Modified Booth Technique and then also it is implemented. The Modified Booth Recoding Technique is mainly used to produce the reduced partial products for the design of many parallel multipliers, which receives the parallel encoding scheme. In this paper the software structure of the Modified Booth Technique is shown by using the schematics. The simulation results are shown by using Xilinx software of Latest Version and ModelSim tools and the results are obtained by running Verilog code. The structure of this adder & multiplier is done by using Hardware Description Language.**

Keywords* - *Modified Booth (MB) Technique, Carry Saving Addition (CSA) and Carry Look Ahead Addition (CLA).

I. INTRODUCTION

Speed Performance multipliers are important parts of digital signal processing systems. The Velocity of multiplication operation is of pleasant importance in DSP as well as in the general intent processors at present. In the prior multiplication was ordinarily applied through a order of adding, Subtracting, and shifting operations. Multiplication will also be considered as a sequence of repeated additions. The number to be delivered is the multiplicand, the number of times that it's introduced is the multiplier, and the effect is the product. Each step of addition generates a partial product. In most computers, the operand normally includes the same number of bits.

When all the operands and values are taken as integers, the product is more commonly twice the area of operands with the intention to keep the understanding content material. This continuous adding procedure that is recommended via the arithmetic definition is slow that means it's most normally replaced by using an technique which takes the use of positional representation. The primary phase is committed to the new collection of partial products, and the second collects and adds them.

II. MODIFIED BOOTH TEHNIQUE

The primary multiplication process is twofold, i.e. generation of partial products and collection of the moved partial products. It's carried out with the aid of the successive Addition's of the columns of the moved partial product collection. The illustration of the multiplicand should be within same column of the shifted partial product matrix. They are then added to kind the product bit for the specified type. Multiplication is thus a multi operand operation. To continue the multiplication to each positive and negative numbers, a simple number approach often is the illustration of bits in two's complement format Multipliers are aided accessories of collective speed performance programs such as FIR filters, microprocessors, digital sign processors, etc. A approach's performance is most often decided through the efficiency of the multiplier when you consider that the multiplier is most commonly the slowest clement in the method. In addition, it is typically the most subject ingesting.

III. EXISTING SYSTEM

In this paper, we discuss about the Add -Multiply units which performs the operation Z=X.(A+B).The existing system of Add-Multiply Operator shown in below diagram takes the input values first and then forwarded to an adder and produces the result of adder as Y=A+B and another input value X both are given to a multiplier circuit in order to get the final output value. The main disadvantage of considering an adder block is that it takes an amount of delay in the crucial way of the Adder-Multiplier circiut.

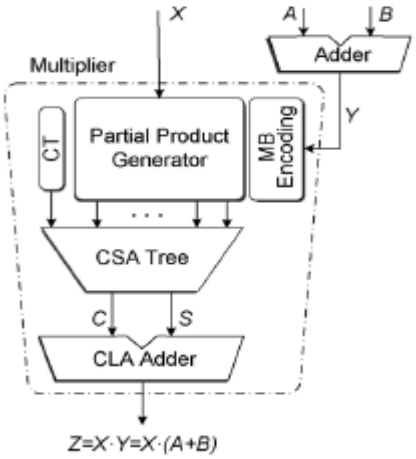


Fig. 1 Existing System of Add-Multiply Operator in Modified Booth representation

Adder:

In this bock we give the two input values as A and B for the addition purpose and generates the result as Y. This result is further given to the multiplier block as input.

Modified Booth Encoding Technique:

This Encoding Technique is a related form of multiplication system which uses the coding technique. It is a reduced negative sign bit radix based en-coding reference form. The possible use of this form is that it decreases the number of partial products generation to exactly half when compared with other radix-2 based system.

Binary			MMB Encoding			carry
Y_{2j+1}	Y_{2j}	Y_{2j-1}	Sign= sj	onej	twoj	
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	1	0	0
0	1	1	0	0	1	0
1	0	0	1	0	1	1
1	0	1	1	1	0	1
1	1	0	1	1	0	1
1	1	1	1	0	0	0

TABLE 1: Modified Booth Encoding Scheme

CSA Tree:

The carry saving addition enters into the type of conditional summing & addition operation. The Conditional summing & addition works based on a related condition. Sum and Carry bits are calculated by assuming input carry as 1 and 0 whatever the input carry bits comes. The carry saving addition process is shown in below example.

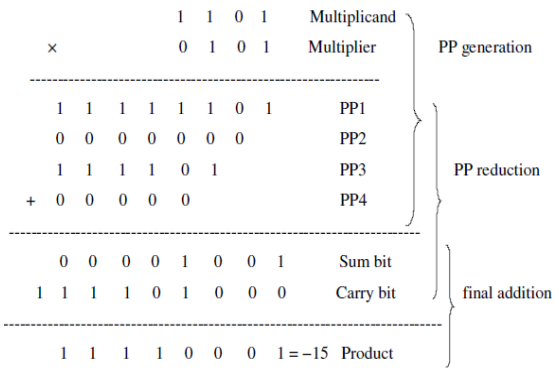


Fig. 2 Example of Carry Save Addition (CSA) Tree

The conventional Carry saving addition circuit has n input bit addition block for the bottom half of the bits i.e. LSB bits and for the top half i.e. MSB bits two n input bit addition blocks. In top adder's one addition block assumes input carry bit as 1 for addition operation and other block assumes input carry bit as 0.

CLA Adder:

A Carry-look-ahead adder (CLA) is a type of adder used in digital logic. By using this adder next further stage has no need to wait for the previous stages output carry. It means that the 3rd stage won't wait for the output carry of 2nd stage. Each stage depends only on the 1st stage carry output. The carry lookahead logic block calculates the input carries for the blocks which are present in next stages. This concept reduces the waiting time for the input carries.

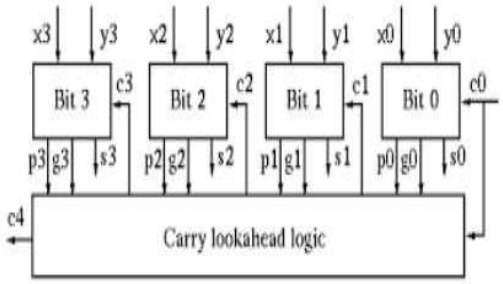


Fig. 3 Logic Diagram of Carry Look Ahead Addition

The propagation delay is reduced in this circuit when compared with Ripple Carry Adder.

IV.PROPOSED SYSTEM

The architecture of proposed system by using fusing technique of Add Multiplier operator with the re-coding scheme of sum by using MB representation is designed in following diagram. In proposed system the adder block is fused in multiplier block by using Fusing Technique which reduces area of complete design.

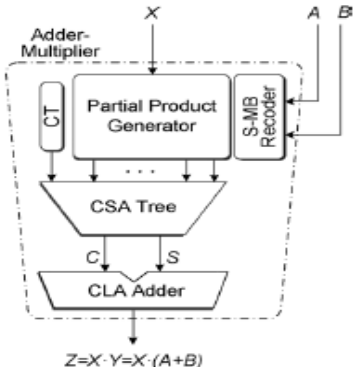


Fig. 4 Proposed design of sum to modified booth recoding scheme

SUM TO MODIFIED BOOTH RECODING TECHNIQUE (S-MB):

In this recoding scheme, we modify the sum of two consecutive bits of the input A with two consecutive bits of the input B into one MB digit Y. As we notice the three bits are integrated in forming a MB digit. The most tremendous of them is negatively weighted whilst the 2 least tremendous of them have optimistic weight. Finally in the form of converting the two combinations of bits in MB form we ought to use signed-bit arithmetic.

S-MB1 recoding scheme:

The first scheme of the implemented recoding technique is referred as S-MB1 Recoding Scheme and is illustrated in detail in below figure for both even and odd bit-width of input numbers. As can be seen in below figure, the sum and carry bits are calculated.

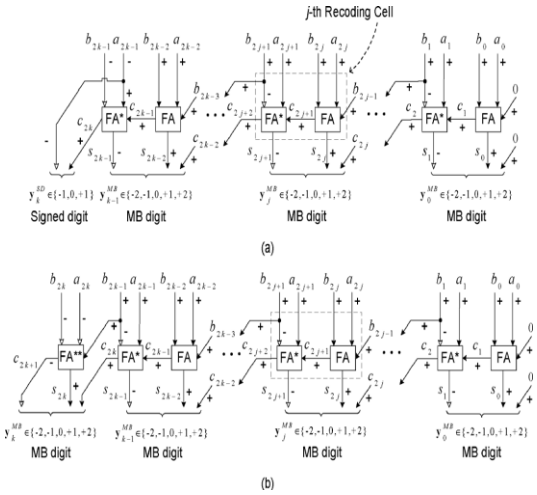


Fig. 5 S-MB1 Technique for (a) even and (b) odd no. of bits.

\S-MB2 Recoding Scheme:

The second technique for the implemented recoding technique, S-MB2, is described in figure for even and odd bit-width of input numbers. It consider the initial values $c_{0,1} = 0$ and $c_{0,2} = 0$. The digits , y_j^{MB} $0 \le j \le k-1$, are formed based on $s_{2j}+1$, s_{2j} and $c_{2j},2$.

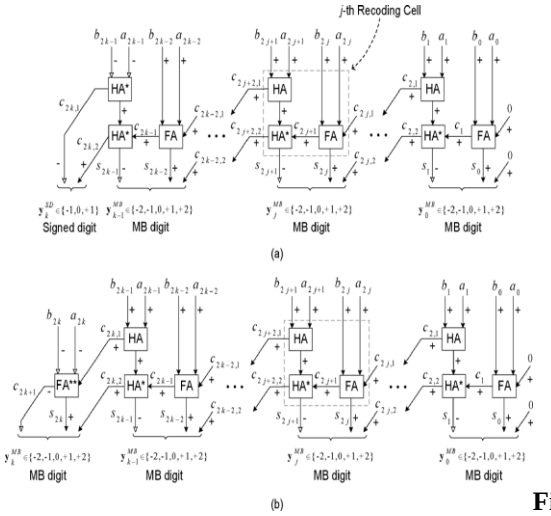


Fig. 6 S-MB2 Technique for (a) even and (b) odd no. of bits

S-MB3 recoding scheme

The third scheme implementing the recoding technique is S-MB3. It is illustrated in detail in for even and odd bit-width of input numbers. It consider that $c_{0,1} = 0$ and $c_{0,2}$. It builds the digits y_j^{MB} , $0 \le j \le k-1$, based on $s_{2j}+1$, s_{2j} and $c_{2j,2}$.

The negatively signed bit s_{2j+1} is produced by a HA** in which drive c_{2j+1} and the output sum (negatively signed) of the HA* of the recoding cell with the bits a_{2j+1}, $b2j+1$ as inputs. The carry and sum outputs of the HA** are calculated.

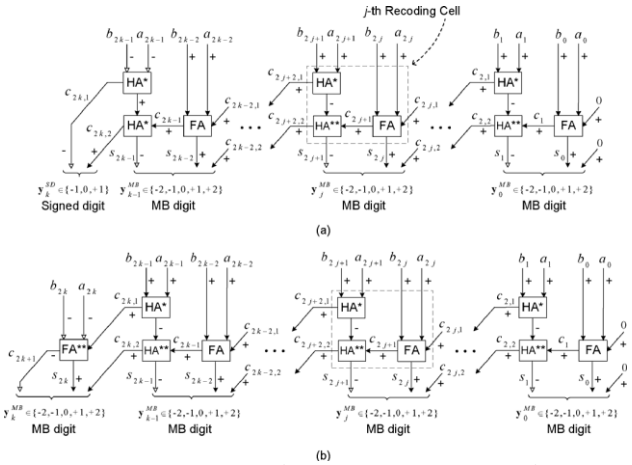
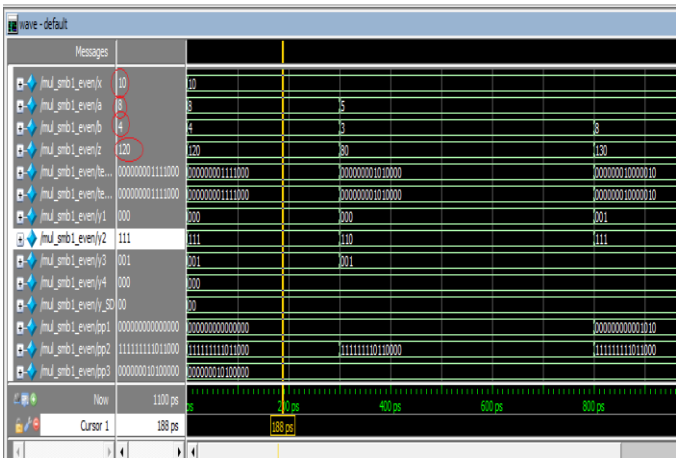


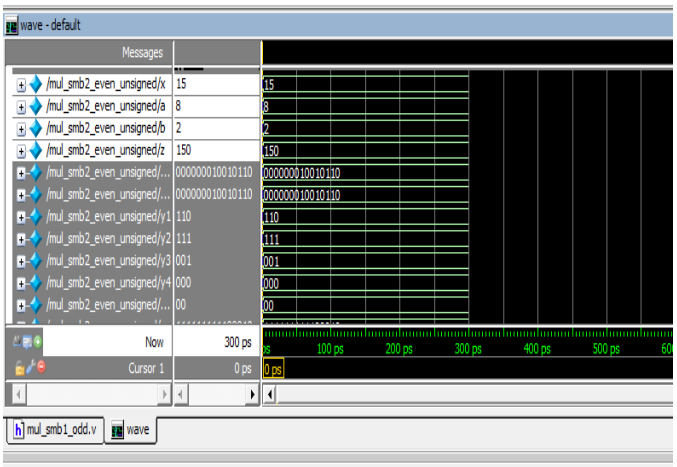
Fig. 7 S-MB3 Technique for (a) even and (b) odd no. of bits

V.SIMULATION RESULTS

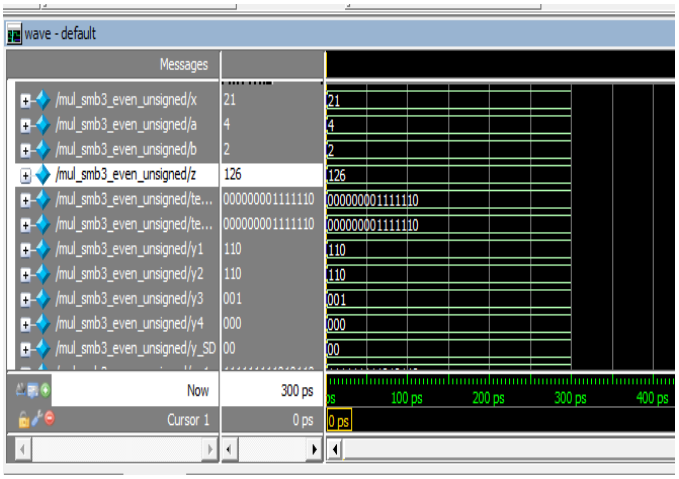
S-MB1



S -MB2



S-MB3



VI.CONCLUSION

Finally I concluded that in this implemented project area of the circuit is reduced by using design of the Fused-Add Multiply (FAM) operator. I advise a structured system for the direct recoding of the sum of two numbers to its Modified Booth form. I discover three substitute designs of the implemented S-MB recoder and compare them to the prevailing ones the implemented recoding schemes, when they are integrated in FAM designs, yield enormous performance upgrades in comparison with essentially the most efficient recoding schemes.

VII.FUTURE SCOPE

The power saving may be increased if the following conditions are considered in the future low power VLSI design. The bit size may be increased i.e., number of bits considered may be increased in the encoding scheme using Modified Booth Technique. The power consumption can be reduced by improving the partial product compression ratio. This concept of Fusing Technique can also be implemented in Radix-8 for area efficiency and low delay.

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N. SHEHANAZ received B.Tech degree in ECE from Rajooli Veera Reddy Padmaja Engineering College for Women, C.K.Dinne, Kadapa in the year 2012 and presently pursuing M.Tech degree in VLSI System Design in Annamacharya Institute of Technology and Sciences, Kadapa. Her research interests include VLSI Chip Design and Communications.

Dr. T. LALITH KUMAR did B.Tech in ECE from S.V University, Tirupati (India) in 1997, M.Tech() from Satyabhama University, Chennai in 2005 and Ph.D in in Feb 2015 from JNTU Ananthapur. He is presently working as Associate Professor in Annamacharya Institute of Technology & sciences, Kadapa. He had a Teaching Experience of 16 years in various Engineering Colleges. He published 10 International Journals and 5 National Journals.